High Efficient Infrared Light Emission from Silicon LEDs

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Cover: Light emission profile (picture made by Victor Zieren) out of a lateral $p^+/p/n^+$ diode realized on SOI wafer under forward bias (*front*) and its schematic structure cross-section (*back*).

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HIGH EFFICIENT INFRARED-LIGHT EMISSION FROM SILICON LEDs

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. W. H. M. Zijm,
on account of the decision of the graduation committee,
to be publicly defended
on Friday, 28th September 2007 at 13.15

by

Hoang Tu
born on 25th December 1974
in Phutho, Vietnam

This dissertation is approved by
the promotor prof. dr. Jurriaan Schmitz and
the assistant promotor dr. Jisk Holleman.

To my parents,
my brother Tung, my sister Trinh,
to my wife Kieu An and to Duy

Contents

Chapter 1

Introduction

Abstract

In this introduction, the main motivations of this work are addressed and following by a short up-to-date overview of all strategies on the field of light emission from silicon. From those the aims of the project are drawn subsequently, and few last sentences present the thesis outline.

1.1 Why Silicon LEDs: interconnect bottleneck

The first commercially available integrated circuit was a silicon chip and it included only a few transistors (in 1958 by Robert Noyce [1], see Figure1.1). Nowadays, after almost a half century of development, where a single chip may contain over one billion transistors, silicon still remains the first choice for integrated circuits [2]. The increasing number of transistors on a single chip requires a corresponding increase of the length of the metal interconnects running in the chip and the capacity for a high rate data transmission ($>$ 10 Gb/s) [3]. Moreover, to be able to integrate a larger number of transistors into the same size of a silicon chip, a smaller cross-section and closer spacing of the connecting metal lines is required. These requirements cannot be fulfilled with the conventional aluminum-based interconnect technology. Using copper and low-k materials instead of the conventional aluminum technology can improve this performance limitation but it can not maintain the continuing track of the scaling progress [4].

To overcome these limitations of the traditional electrical interconnects, 3D integration is suggested where the interconnects run vertically to transistors on different levels [5] [6] but also optics has been proposed as a potential solution. Using photons instead of electrons for data transmission, limitations of electrical interconnects can be solved. On the other hand, silicon was shown to be a

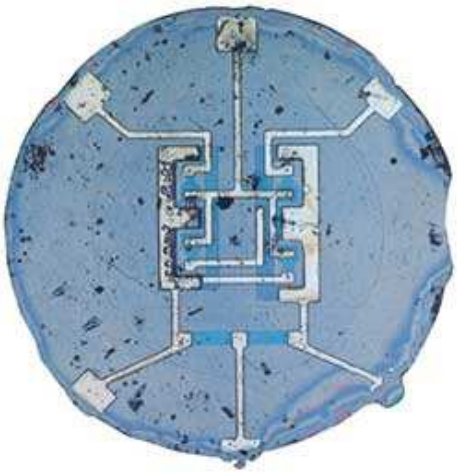

Figure 1.1: The first Si commercially integrated circuit (Si-IC) by Robert Noyce [1].

very good candidate as wave-guide because silicon is a tight optical confinement medium due to the large difference of refractive index between silicon and SiO_2 [7]. However, until now an efficient light source being suitable for optical interconnects has been made from III-V materials and not from silicon [8]. It is feasible to directly grow III-V semiconductor materials on silicon substrates. But this approach so far has suffered from process incompatibility with standard Si CMOS technology, making it a complicated and expensive solution. Thus, silicon is again the most attractive choice for low-cost photonic integrated circuits. As a result, seeking for an efficient silicon light source, which can be made by an IC compatible process, still remains a challenging research subject for scientists around the world. Once this efficient silicon light emitting device is made, it will be a large breakthrough for a new generation of optoelectronics circuits.

1.2 Silicon photonics: state-of-the-art

Despite the fundamental limitations of silicon in light emitting probability because of its indirect band-gap [9], different strategies have been intensively studied in order to investigate emission from silicon [10–27]. These strategies can be divided into: nanometer-size silicon emitters; rare-earth doped nanocrystalline silicon; SiGe LEDs; bulk Si LEDs and SOI LEDs. In 2003, overviews of these research topics by different approaches were collected and published in [28]. Here we just give an additional overview of the new progress on each topic.

1.2.1 Nanoscale dimension Silicon LEDs

The topic of luminescence from nanocrystalline Si (nc-Si) becomes attractive because nc-Si can emit visible light due to its widened bandgap. The nc-Si can e.g. be obtained from porous silicon. The highest power efficiency obtained from porous silicon LEDs has still been at 1 % since 2000 [10]. Many efforts have focussed to improve the stability of this type of LEDs, and recently Gelloz reported that by using the high pressure water vapor annealing technique the stability increased up till several months [11]. However, further stability improvement is being searched for.

Nc-Si can be embedded in a dielectric (such as SiO_2 and Si_3N_4) by Si implantation into SiO_2, by annealing of silicon-rich SiO_2 or annealing of amorphous Si/SiO_2 superlattices or by CVD of nuclei. Many of such materials showed high efficiency [12] [13] in the case of photoluminescence (PL) but poor efficiency in the case of electroluminescence (EL) [14] [15]. Thus, the real application of these approaches is still questionable.

Together with Si nanocrystals (quantum dots), there were recently reported results on luminescence from nanowires (quantum wires) [16] [17] but no information of efficiency was shown; and only PL from quantum wells was presented in [18]. Too low efficiency can be considered the main limitation of the luminescence from these Si quantum wires and quantum wells.

1.2.2 Rare-earth doped silicon LEDs

When a rare-earth element (Gd, Yb, Tb, Er) is doped into Si LEDs, the LEDs can emit violet (316 nm), visible light (850 nm) or infrared light (1500 nm) depending on the excitation state of charges between Si atoms and doped rare-earth atoms. The mechanism behind the light generation is excitation of the rare-earth atoms by hot electrons. The incorporations of Er/Tb and silicon enhanced the light emitting efficiency. The external quantum efficiency was typically 10 % from MOS structures where Er/Tb atoms were embedded in a thin SiO_2 layer [19]. But the relatively low solubility of these elements in crystalline silicon limits the power efficiency of this type of LEDs.

The most attractive rare-earth element in this topic is Erbium because of its telecommunications wavelength emission and its CMOS-compatible process [20]. Again, the limitations in stability and operation speed are still the main problems of this approach.

1.2.3 SiGe LEDs

The SiGe LED is attractive because SiGe can be grown directly on a silicon substrate by molecular beam epitaxy or by LPCVD and the fabrication process is IC compatible. The most prospective SiGe light sources are the quantum cascade Si/SiGe structures. However, because of the large mismatch between Si and Ge lattices, in order to avoid the formation of dislocations only a small number of quantum wells can be grown. Thus the total thickness of the quantum cascade must be kept below the critical thickness [21]. While a sufficient gain for laser operation requires a large number of periods of successive cascades, then, even though a lot of effort has been put in this subject, a SiGe laser is still missing [22].

1.2.4 Bulk Si LEDs

Bulk Si LEDs with high efficiency were fabricated and reported in literature [23–26]. In [23] it was claimed that the high efficiency observed in their LEDs was caused by the carrier confinements due to local potential barriers introduced by the stress field around the formed dislocation loops. However, this hypothesis is strongly debated [24] [25].

The key factor of the observed high efficiency of bulk Si LEDs as demonstrated through different approaches [24–26] seems to be the high quality of Si material. Still, limitations for bulk Si LEDs are, however, low switching speed and lack of spatial confinement of the generated light.

1.2.5 SOI LEDs

The SOI technology is seen as a powerful platform for modern electronics integrated circuits and also for photonic integration [7]. The fabrication of a lateral LED in thin-film high quality SOI material has a few advantages over bulk silicon, such as higher optical switching speed with lower power consumption, better options for integration and coupling of the light into waveguides.

However, to date, the highest reported efficiency of SOI LEDs is two orders of magnitude lower than in bulk silicon LEDs [27]. The main reason for this low efficiency is the large fraction of non-radiative recombination processes occurring at the interfaces and at the junctions over the competitive radiative process.

1.3 Aims of the project

This project aims to realize Silicon Light Emitting Diodes (Si-LEDs) on high-quality silicon-on-insulator (SOI) material to circumvent certain disadvantages of

electroluminescent devices fabricated in bulk silicon technology. We intend to create a compact and high switching speed light source which enables the possibility for on-chip optical integration.

The project proposes to make light emitting devices in silicon which can emit a usable amount of light, i.e., the devices are highly efficient emitters. When electrons and holes are confined within a silicon volume, they will have more probability to recombine in the confining volume rather than at the contacts and thus the emission efficiency would be enhanced. This confinement can be reached by creating a material with a higher band gap between the contacts and the volume. The potential barrier implemented in this carrier confinement can be created by band-gap widening effects when the SOI layer becomes $\sim$ 5–10 nm thick.

1.4 Outline of thesis

In this thesis, investigations on near-infrared light emission by means of electroluminescence from silicon diodes are described.

The fundamental physics of internal and external efficiency of the fabricated devices are shown in chapter 2. The model used to calculate the relationship between internal and external efficiency is also proposed in this chapter. The reabsorption effects of Si wafer on the position of the emission spectral peak were investigated theoretically.

In chapter 3, the descriptions of equipment used for both electrical and optical measurements in this work are presented. The calibration of the optical system was carried out in our laboratory. The calibration procedures and the equipment used for this calibration can also be found in this chapter.

In chapter 4, the obtained results from a series of experiments investigating the infrared light emission from bulk silicon with dislocation loop engineering are exhibited. The work mentioned in chapter 4 was extended in a full range (both EL and PL) to investigate a complete luminescence picture of the dislocation loop engineering devices, which can be found in chapter 5.

In chapter 6, we present our important achievements from the fabricated LEDs using SOI technology. The lateral LEDs were made with many variations in structures to explore the efficiency improvement resulted from the implemented carrier confinement effects.

Finally, the conclusions and some recommendations are given in chapter 7.

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Chapter 2

Internal and External Efficiency of Silicon LEDs

Abstract

In crystalline silicon the direct band-to-band recombination between electrons and holes is only a small fraction of the total of recombination processes. The relationship between the competing radiative and non-radiative recombination was investigated and is presented in this chapter. The highest possible efficiency of the light-emitting process in silicon can be predicted quantitatively. A few methods to enhance the internal emission efficiency by reducing the non-radiative recombination rate are suggested. Rules from optics show that only a very small fraction of the generated light has a chance to escape from internal reflection/absorption. The relationship (extraction coefficient) between the external efficiency and the internal efficiency of the realized diodes was calculated. Some proposals to improve the efficiency of Si LEDs are presented.

Introduction

In a Silicon light emitting device, the internal efficiency of the luminescence process is determined by all physical recombination processes occurring within the device structure. The internal efficiency is determined by the ratio of the radiative recombination rate to the total recombination rate occurring in the emitting structure. The total recombination rate includes the radiative recombination together with all non-radiative recombination processes such as Auger-, Shockley-Read-Hall-, and surface/interface recombination. The internal efficiency can be extracted from the external efficiency of the luminescence process from the Si light emitting device which is determined by the way how the emitted light penetrates to the outer world and how the externally emitted light is collected and processed.

There are many different available techniques being used for external observation of luminescence from a light source and leaves us with the questions on how much light has been emitted internally inside the device body? Which fraction of the emitted light could get out and reach the detector? How about the possibility to improve the internal efficiency of the light sources?

In this chapter we will deal with these questions and then give some calculation models applying for our fabricated emitting structures.

2.1 Radiative and non-radiative recombination in a Si-LED

2.1.1 Recombination mechanisms

There are several mechanisms for the recombination of electrons and holes in a semiconductor device. An electron can either recombine directly with a hole or via a trap. The result of these transitions can be phonons, photons or excited carriers. The probability for such processes depends not only on the number of available electrons and holes or the number of traps but also on their states as well as on the band-structure of the semiconductor. Since silicon has an indirect band-gap, where the bottom of the conduction-band and the top of the valence-band is located not at the same momentum value, the recombination of an electron from the conduction-band with a hole in the valence-band needs assistance of a phonon in order to fulfill the requirement of energy and momentum conservation [1]. Thereby, the probability for a direct band-to-band transition between electrons and holes in silicon is not so high compared to that in a direct band-gap material. Or in other words, the radiative recombination efficiency of silicon is relatively low. In this section we present some calculations on the fraction of

radiative and non-radiative recombination occurring internally in a Si-LED as a function of injection level, i.e., excess carrier concentration, at different densities of trap-states in the silicon-volume and at the interfaces. We will then give some predictions of the highest possible efficiency for a Si-LED.

The physical mechanisms of recombination processes can be divided into four main categories: band-to-band-, Shockley-Read-Hall-, Auger- and interface recombination [2]. The band-to-band recombination process generates photons (light) and the others are non-radiative events. An exception has to be made for the so-called D-line emission in silicon which occurs through dislocation related states [3]. One could consider this type of light emission as a special form of . In chapter 5 we address the issue of the D-line emission in more detail. At room temperature, however, the D line emission is of minor importance.

We further focus on the most important process for a light emission which is the radiative recombination between conduction band electrons and valence band holes. Since we consider only the direct transition process, where both electrons and holes must be present simultaneously, the radiative recombination rate is proportional to both electron and hole concentrations, i.e., proportional to their product, and it can be expressed as

$$R_{\mathrm{BB}} = B_{\mathrm{rad}} \left(\mathrm{n\,p} - \mathrm{n_i^2} \right) \tag{2.1}$$

where $n = n_0 + \Delta n$ and $p = p_0 + \Delta p$ are electron and hole concentration at nonequilibrium condition, with the equilibrium and excess electron and hole concentration are n_0, p_0, Δn, and Δp respectively, n_i is the intrinsic carrier density, and the proportionality constant B_{rad} is the radiative band-to-band recombination coefficient.

For the case of high injection level, the excess carrier concentration is much larger than the equilibrium carrier concentration, i.e., $\Delta n \gg n_0$, $\Delta p \gg p_0$. Further at high injection n = p, the radiative recombination rate (2.1) can be re-expressed as

$$R_{\mathrm{BB}} = B_{\mathrm{rad}} \cdot \mathrm{n}^2. \tag{2.2}$$

For crystalline silicon, it is known from the work by Schlangenotto *et al.* [4] that the radiative recombination coefficient B_{rad} is enhanced by the Coulomb attraction between electrons and holes at low carrier concentration and thereby the Coulomb interactions constitutes a dominating factor in the recombination rate. This theory was recently strengthened by a new approach presented in [5]. These observations pointed out that B_{rad} depends on the injection level (i.e., the excess carrier concentration) and the lattice temperature. At high injection level there is a strong mutual screening of charges which reduces the radiative recombination constant B_{rad}.

The *Shockley-Read-Hall* (SRH) model describes the generation-recombination of electrons and holes through traps (or defects) in the semiconductor crystal.

These defects can be unwanted contaminants, e.g. iron, interstitials, vacancies, dislocations, which were introduced in the device structure during the fabrication process or during crystal growth. Such defects create one or more energy levels within the band-gap of the semiconductor. If this energy level is close to the middle of the band-gap, it will be an efficient recombination center for carriers. In fact, a semiconductor always contains some impurities/defects therefore the SRH recombination is always active.

In silicon, the net SRH recombination rate through a deep level with trap-energy of $\mathrm{E_t}$ and trap concentration of $\mathrm{N_t}$ is given by

$$R_{\mathrm{SRH}} = \frac{v_{\mathrm{th}}\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}N_{\mathrm{t}}(\mathrm{pn} - \mathrm{n_i^2})}{\sigma_{\mathrm{p}}\left[\mathrm{p} + \mathrm{n_i e^{(E_i - E_t)/kT}}\right] + \sigma_{\mathrm{n}}\left[\mathrm{n} + \mathrm{n_i e^{-(E_i - E_t)/kT}}\right]} \tag{2.3}$$

where v_{th} is the thermal velocity of carriers; σ_{n} and σ_{p} are the capture cross-sections of the recombination center for electrons and holes respectively; $\mathrm{n_i}$ is the intrinsic carrier density and E_{i} is the intrinsic Fermi level; n and p are electron and hole concentrations respectively; k is Boltzmann's constant; T is the absolute lattice temperature.

In its simplified form where we assume that the trap level is at midgap, i.e., $E_{\mathrm{t}} \approx E_{\mathrm{i}}$, and where we assume that the product of capture cross-section and thermal velocity for electrons and holes is the same, and when we further assume that the diode operates in the regime of high injection level where n = p, i.e., the electron and hole concentration are equal, and thus pn = $\mathrm{n^2} \gg (\mathrm{n_i})^2$, the rate of SRH recombination $\mathrm{R_{SRH}}$ is then given by the simplified equation:

$$R_{\mathrm{SRH}} \simeq \frac{1}{2}\sigma\upsilon N_{\mathrm{bt}}\,\mathrm{n} \tag{2.4}$$

where σ is the effective capture cross section for electrons and holes, υ is the effective thermal velocity, and $\mathrm{N_{bt}}$ is the concentration per $\mathrm{cm^3}$ of bulk recombination centers. By setting $\sigma\upsilon N_{\mathrm{bt}} = (\tau_{\mathrm{SRH}})^{-1}$ with τ_{SRH} is the Shockley-Read-Hall lifetime, Eq. (2.4) can be written as $R_{\mathrm{SRH}} = \frac{1}{2}(\tau_{\mathrm{SRH}})^{-1}\,\mathrm{n}$.

The second non-radiative process is surface/interface recombination. Because of the abrupt discontinuity of the lattice structure at the interface, the band diagram will need to be modified at the semiconductor surface. Thus, a large number of localized energy states may be introduced within the forbidden gap of the semiconductor at the surface/interface region. Generation-recombination via surface states occurs with a similar process as for bulk states, therefore a similar equation holds for surface recombination rate R_{s} per $\mathrm{cm^2}$:

$$R_{\mathrm{s}} \simeq \frac{1}{2}\sigma_{\mathrm{s}}\upsilon N_{\mathrm{st}}\,\mathrm{n} \tag{2.5}$$

where σ_{s} is the capture cross-section of carriers at the surface state; N_{st} is the surface state density per cm^2. In this equation, defining surface or interface recombination velocity as s = $\sigma_{\mathrm{s}} \upsilon N_{\mathrm{st}}$, we have

$$R_{\mathrm{s}} = \frac{1}{2}\mathrm{s} \cdot \mathrm{n}. \tag{2.6}$$

The reported experimental data in [2] showed that the surface recombination rate decreases when increasing the injection level. It is important to note that the surface recombination is more complicated than the SRH recombination in the bulk, because it depends not only on the density of surface-states or interface-traps, but also on the state of the surface [6] [7], i.e., accumulation, inversion or depletion.

The third important non-radiative recombination is Auger recombination. Auger recombination is a three body collision where an electron and a hole recombine, the released energy is transferred to another electron or hole. In silicon which has an indirect band-gap in order to preserve momentum also a phonon is involved in this process. The net Auger recombination rate can be expressed generally as

$$R_{\mathrm{Auger}} = C_{\mathrm{n}}\left(\mathrm{pn}^2 - \mathrm{nn}_{\mathrm{i}}^2\right) + \mathrm{C_p}\left(\mathrm{np}^2 - \mathrm{pn}_{\mathrm{i}}^2\right) \tag{2.7}$$

where C_{n} and C_{p} are the Auger coefficients for e-e-h and h-h-e recombination where e stands for electron and h for hole, respectively, and they can be experimentally extracted for each identical material. For silicon at room temperature it is found that $C_{\mathrm{n}} = 2.8 \times 10^{-31}$ cm^6/s and $C_{\mathrm{p}} = 0.99 \times 10^{-31}$ cm^6/s [8].

In high injection condition, where n = p the Auger recombination rate can be reduced to

$$R_{\mathrm{Auger}} = \left(C_{\mathrm{n}} + C_{\mathrm{p}}\right)\mathrm{n}^3 = \mathrm{C_a} \cdot \mathrm{n}^3 \tag{2.8}$$

with $C_{\mathrm{a}} = C_{\mathrm{n}} + C_{\mathrm{p}}$ is the ambipolar Auger recombination rate constant.

It is also observed that the Auger coefficient decreases when increasing the injection level [9] or decreasing the temperature [10].

Within the four presented recombination events, the SRH and surface recombination rate depend strongly on the density of recombination centers and their capture cross-section. They are further linear with the injection level. The Auger recombination rate is proportional to the cubic of carrier concentration and the band-to-band recombination is proportional to the square of carrier concentration. It is easy to signify that at a lower injection level the SRH transition keeps a more important role over the others, while at higher carrier density the Auger transition controls the effective carrier-lifetime.

2.1.2 Internal efficiency in bulk Si LEDs

Next we present some calculations on the internal efficiency of Si light sources at room temperature as a function of the injection level in the range of $10^{15} - 10^{20}$ /cm^3. For the Band-to-Band recombination we use Eq. (2.2) with the radiative recombination coefficient $B_{rad} = 9.5 \times 10^{-15}$ cm^3/s. The dependence of B_{rad} on the carrier concentration is also taken into consideration [5]. The Auger coefficient used in our calculations also depends on the excess carrier density [9]: when the excess carrier concentration is less than 10^{15} /cm^3 we have $C_n = 2.8 \times 10^{-31}$ cm^6/s and $C_p = 0.99 \times 10^{-31}$ cm^6/s and as the injection level increases the Auger coefficient will decrease according to $C_a = 3.79 \times 10^{-31} \left(\frac{\Delta n + 3.8 \cdot 10^{17}}{\Delta n + 6 \cdot 10^{16}}\right)$ cm^6/s. The SRH recombination rate was calculated for two different trap-density levels, $N_t = 10^{10}$ /cm^3 and $N_t = 10^{14}$ /cm^3 [2] with the assumption of uniform trap distribution within the silicon volume and an equal capture cross-section for electrons (σ_n) and holes (σ_p) of 10^{-15} cm^2. Whereas the surface recombination rate was chosen either at 1 cm/s or at 10 cm/s [13].

The internal efficiency was obtained by the ratio of the radiative recombination rate and total recombination rate of all recombination processes. In the case of photoluminescence (PL), where excess electrons and holes are generated by external illuminations, photons are emitted in the absence of the electrical contact, then the expression for the internal PL efficiency is

$$\eta_{PL} = \frac{R_{BB}}{R_{BB} + R_{SRH} + R_{Auger} + R_{s,V}} 100\ \%. \tag{2.9}$$

with $R_{s,V} = R_s \left(A_{ox}/V_{dev}\right)$ where A_{ox} is the total oxide area and V_{dev} is the device volume.

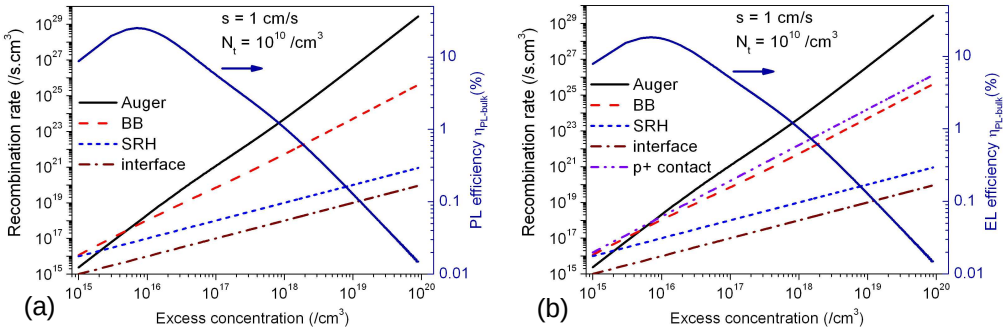


Figure 2.1: All recombination mechanisms and the internal quantum efficiency as a function of excess carrier concentration for: (a) PL and (b) EL from bulk silicon.

We can do the same calculations for the case of electroluminescence. Compared to photoluminescence we have to take into account the recombination in

the p^+/n contact (or n^+/p contact). The dominant mechanism for recombination at the p^+ and n^+ contact at high injection level is Auger recombination due to the high carrier concentration in these contacts. Further the carrier concentration at high injection level in a p^+/p/n^+ diode is not uniform but shows a bath-type shape with an enhanced carrier concentration at the contacts [14]. And the minority carrier concentration in the p^+ and n^+ contacts is further enhanced due to band-gap narrowing in these contacts. Due to a high recombination rate at the contacts the minority carriers quickly disappear here. The contact recombination rate R_{contact} can be obtained by applying the Auger recombination mechanism for the contact volume. Like surface recombination the recombination at the contacts can be considered as a heterogeneous process and its influence will become very important when the total recombination in the contacts becomes larger than the bulk recombination. The EL quantum efficiency for the bulk silicon LEDs can be expressed as

$$\eta_{\mathrm{EL}} = \frac{R_{\mathrm{BB}}}{R_{\mathrm{BB}} + R_{\mathrm{SRH}} + R_{\mathrm{Auger}} + R_{\mathrm{s,V}} + R_{\mathrm{contact,V}}} 100\%. \qquad (2.10)$$

with $R_{\mathrm{contact,V}} = R_{\mathrm{contact}}\,(A_{\mathrm{j}}/V_{\mathrm{dev}})$, where A_{j} is the total area of the junctions.

Figure 2.1a shows the dependence of all recombination processes and the internal efficiency on the excess carrier density for PL from a 500 μm thick silicon wafer at trap density level of $N_{\mathrm{t}} = 10^{10}$ /cm^3 and for the surface recombination velocity of 1 cm/s. We see that in the case of PL from a large volume of silicon wafer with low trap density ($N_{\mathrm{t}} = 10^{10}$ /cm^3), the highest internal efficiency of 26 % (the same range as in [11] & [12]) can be reached at excess carrier densities of $\sim$10^{16} /cm^3. Likewise for the case of electroluminescence (EL), the dependence of the recombination rate and efficiency on the excess carrier density from bulk silicon can be seen in Figure 2.1b.

An efficiency comparison of PL and EL from bulk Si with different interface recombination velocities and different trap densities is presented in Figure 2.2. We see that the efficiency peak decreased when increasing the interface recombination velocity to 10 cm/s. But when the trap density increases to $N_{\mathrm{t}} = 10^{14}$ /cm^3, the efficiency dramatically drops to 0.4 %. This drop strongly indicates that the purity level (or impurity concentration) of the silicon material is a very important factor in the emission efficiency.

It is also clearly shown in Figure 2.2 that the non-radiative recombination component occurring at the junctions has quite a large influence on the EL efficiency of the bulk silicon LEDs. Similar to PL, the same strong effect of the trap density on the EL efficiency from bulk silicon can be predicted.

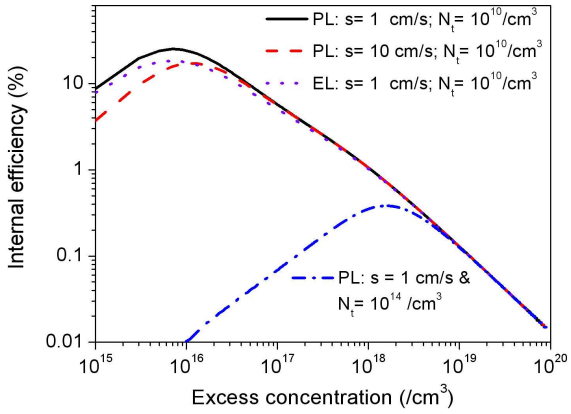


Figure 2.2: Comparison between PL and EL efficiencies, and between PL efficiency at different interface recombination velocities or at different trap densities.

2.1.3 Internal efficiency in SOI-LEDs

Now we shall consider the luminescence from silicon-on-insulator (SOI) material. In SOI material, the silicon emitting volume is just within a thin-film of a few hundreds of nanometers thick. Therefore, the relative ratio between the boundary area and the volume becomes very large compared to the bulk silicon ($\sim$500 μm thick). We do the same internal-efficiency calculations for SOI material with thickness levels of 150 nm (as in our realized devices) and 2 μm whereas all other parameters are the same as for the case of bulk silicon.

In case of PL from SOI wafer ($\eta_{\mathrm{PL-soi}}$) presented in Figure 2.3a, we clearly see a stronger influence of luminescence efficiency on recombination rate at surfaces/interfaces referred to that from the bulk silicon. At the trap density of 10^{10} /cm^3 and the interface recombination velocity of 1 cm/s, it is not possible to obtain a PL efficiency higher than 2.5 % from the 150 nm thick SOI thin-film. However, when increasing the SOI thickness to 2 μm, we are able to extend this efficiency upto 6 %. Theses values of efficiencies are even lower if the 10 cm/s surface recombination velocity is taken into account.

The EL efficiency $\eta_{\mathrm{EL-soi}}$ from SOI p$^+$/p/n$^+$ diodes as a function of injection level can be seen in Figure 2.3b. In this situation, the non-radiative recombination occurring at the two junctions (p$^+$/p and n$^+$/p) was also taken into consideration. The peak of $\eta_{\mathrm{EL-soi}}$ is just 0.4 % at the excess concentration of 2×10^{17} /cm^3 for the 150 nm thick SOI with s = 1 cm/s. Whereas, with the 2 μm SOI material, this efficiency peak is about 0.8 %. For 150 nm and s = 10 cm/s, the efficiency even drops below 0,1 %. Compared to PL data, we see that the EL efficiency is almost one order smaller due to the non-radiative recombination at the junctions. It clearly indicates that the non-radiative recombination at these two junctions

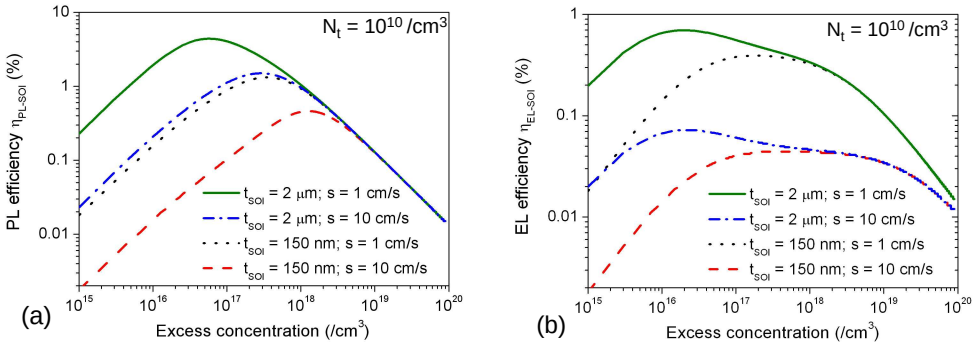


Figure 2.3: Calculation of quantum efficiency for (a) PL and (b) EL from SOI.

is extremely important for SOI LEDs. We believe that this is the main reason for the very low EL efficiency reported so far for a SOI LED [15]. If there is a barrier which can be used to block electrons from reaching the p^+/n junction or to block holes from reaching the n^+/p junction, it will provide a large potential improvement of the EL efficiency from SOI LEDs.

From the obtained data based on the fundamental calculations above we believe that the purity level of silicon is the important parameter for silicon light emitting devices for both bulk and SOI material. Moreover, in the case of SOI LEDs, suppression of the non-radiative recombination occurring at the interfaces and at the junctions is a key issue. In the following chapters we present how we dealt with these essential findings and the obtained experimental results.

In the next sections of this chapter we deal with the relationship between the internal and external efficiency of the bulk silicon and SOI LEDs.

2.2 The relationship between internal and external efficiency

2.2.1 Theory of reflection and transmission from multiplelayer thin-films

Every medium has typical characteristics regarding reflection, transmission and absorption of incident light waves. The refraction coefficient (or real part of the refractive index), n, and extinction coefficient (or imaginary part of the refractive index), k, are referred to as optical constants of a medium. These optical constants are a function of the wavelength λ. The *Kramers-Kronig* relation defines the (complex) refractive index *N* as

$$N(\lambda) = n(\lambda) - ik(\lambda). \tag{2.11}$$

When a light-wave imposes to an interface between two media (often dielectrics), generally it will split into three parts: light reflected back into the incident medium; light transmitted through the second medium; and light absorbed in the second medium. The relative fraction between these parts depends on the refractive index of the two media and the incident angle of the light ray. The coefficient of reflection, $\rho(\lambda)$, and transmission, $\sigma(\lambda)$ at an interface of two media depends on the difference in the refractive index of these two media at each side of that interface, whereas the extinction coefficient (*k*) determines the absorption coefficient $\alpha(\lambda)$. The relationship between the incident angle (θ_0) and the transmittance angle θ_1 of the light ray at the interface is expressed by Snell's law:

$$n_0 \cdot \sin\theta_0 = n_1 \cdot \sin\theta_1 \tag{2.12}$$

where n_0 and n_1 is the refractive coefficient of incident medium and transmission medium respectively, corresponding to this wavelength. The absorption and extinction coefficient of a material have a relation as

$$\alpha\left(\lambda\right) = \frac{4\pi k}{\lambda} \qquad [\mathrm{cm}^{-1}]. \tag{2.13}$$

When a light ray goes from a higher- to lower-index medium, it may fulfill the condition of the total internal reflection if the incident angle is larger than a critical angle. The critical angle can be calculated from (2.12) by setting $\theta_1 = 90^\circ$ which results into $\theta_{\mathrm{crit}} = \arcsin(\frac{n_1}{n_0})$. In our experiments, the light was generated in silicon (a high refractive index material) while the surrounding medium has a lower refractive index. Therefore in general the critical angle is very small. All the light (generated from the light source) being within a cone with an apex-angle of 2 x θ_{crit} can escape to the surrounding medium, whereas the light out of the cone is confined in silicon by multiple reflections. This cone is defined as the *escape cone*, and in our experiment the escape cone is small because of the small critical angle.

If we consider the energy relationship between these parts of the incident wave with amplitude E_0, then the reflected wave and transmitted wave will have the amplitude of ρE_0 and σE_0. And the reflectance *R* of the material is equal to ρ^2 [16], where ρ can be expressed as

$$\rho = \frac{N_0 - N_1}{N_0 + N_1}. \tag{2.14}$$

According to (2.14), ρ is negative when the light wave goes from a lower- to higher-index medium, and this signifies a 180° phase change for the reflected wave.

Let's consider a general situation where a light wave hits to a multiple-layer film including q interfaces. In 1937, Rouard demonstrated that a multiple-layer film can be analyzed by representing the j$^{\text{th}}$ layer by a 2×2 matrix M_{j}:

$$M_{\text{j}} = \begin{pmatrix} \cos\delta_{\text{j}} & \frac{i\sin\delta_{\text{j}}}{N_{\text{j}}} \\ iN_{\text{j}}\sin\delta_{\text{j}} & \cos\delta_{\text{j}} \end{pmatrix} \tag{2.15}$$

where the phase-shift is defined as

$$\delta_{\text{j}} = \frac{2\pi}{\lambda} N_{\text{j}} t_{\text{j}} \cos\theta_{\text{j}} \tag{2.16}$$

with t_{j} and N_{j} is thickness and refractive index of the j$^{\text{th}}$ layer.

The combination effect of these layers can be obtained just by simply taking the product of their represented matrices. The top and bottom media can be displayed respectively by two special matrices $\begin{pmatrix} N_0 & -1 \\ N_0 & +1 \end{pmatrix}$ and $\begin{pmatrix} 1 \\ N_f \end{pmatrix}$.

The reflectance and transmittance of the multiple thin-film is given by

$$R = \left(\left|\frac{a}{b}\right|\right)^2, \qquad T = \frac{4 \cdot N_0 \cdot N_f}{b\bar{b}} \tag{2.17}$$

where *a* and *b* are obtained from

$$\begin{pmatrix} a \\ b \end{pmatrix} = \begin{pmatrix} N_0 & -1 \\ N_0 & +1 \end{pmatrix} \prod_{j=1}^{q} \begin{pmatrix} \cos\delta_{\text{j}} & \frac{i\sin\delta_{\text{j}}}{N_{\text{j}}} \\ iN_{\text{j}}\sin\delta_{\text{j}} & \cos\delta_{\text{j}} \end{pmatrix} \begin{pmatrix} 1 \\ N_f \end{pmatrix}. \tag{2.18}$$

Since Si and SiO_2 are two very important materials for our applications we treat, in the next section, their optical constants as a function of wavelength at room temperature (300 K).

2.2.2 Optical constants of Si and SiO_2

The extinction- and refraction -coefficient at 300 K can be extracted from Eq. (A.5) and Eq. (A.13) respectively (see Appendix A). The dependence of these constants on the wavelength is presented in Figure 2.4). The absorption coefficient of SiO_2 is negligible, because its extinction coefficient is very small (Figure 2.4). The extinction coefficient for Si is quite large and changes with the carrier concentration. The absorption of heavily doped silicon was characterized in [17] and a small difference of the absorption coefficient between n-type and

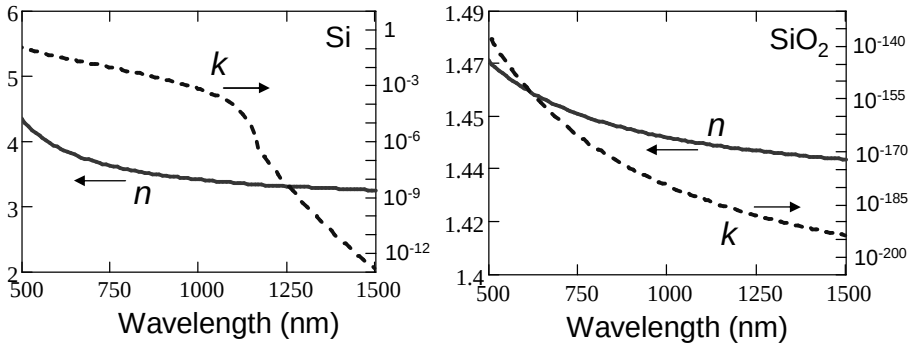


Figure 2.4: Refraction and extinction coefficient of intrinsic crystal Si (left) and SiO_2 (right) at 300 K versus wavelength.

p-type silicon was observed but in our calculation we ignored this difference. The absorption edge (below the band-edge) of intrinsic silicon was extracted from the measurements by Keevers and Green [18], whereas that of SiO_2 was calculated by the Urbach theory [19]. Figure 2.5a shows the absorption coefficient of intrinsic silicon and with different doping concentrations at 300 K.

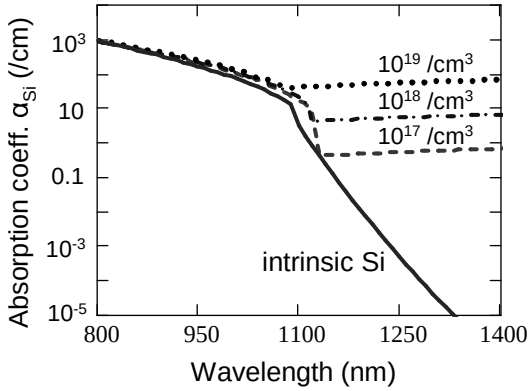


Figure 2.5: Absorption coefficient of intrinsic Si and heavily doped Si as a function of wavelength at 300 K. Absorption coefficient depends on n-type or p-type dopants but the calculation data shows the difference is small then in this calculations we ignore this difference.

Together with Si and SiO_2, the optical constants of aluminum is also a necessary parameter because in our light-emitting structures a layer of 1 μm Al was evaporated on the backside of the wafer in order to create a better electrical contact. However, in the wavelength range of interest (800–1500 nm) its optical constants do not vary much [20]. We used a mean value for both refraction and extinction coefficients in our calculations: $n_{Al} = 1.23$ and $k_{Al} = 10.25$.

2.2.3 Lambertian emission pattern and extraction coefficient

In our light sources the generated light propagates isotropically within the silicon region, which is normally covered by a thermally grown SiO_2 layer. The generated light within the escape cone will pass through the top SiO_2 layer and emit into the outer world (air). The light rays follow Snell's law (see Figure 2.6). The relation between θ_0 and θ_r can be derived using eq. (2.12). For small incident

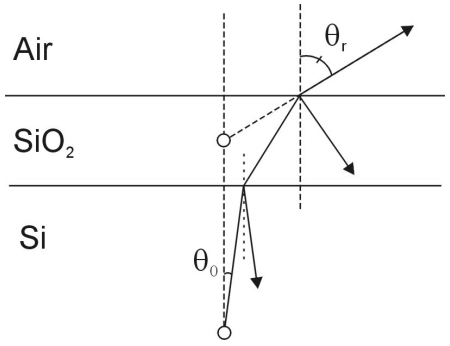


Figure 2.6: Snell's law for a planar LED.

angle (where $\sin\theta_0 \sim \theta_0$ or $\cos\theta_0 \sim 1$), it reduces to

$$n_{\mathrm{Si}} \cdot \theta_0 = n_{\mathrm{air}} \cdot \sin\theta_r. \tag{2.19}$$

The light generated within an angle element $\mathrm{d}\theta_0$ in silicon will be transmitted in air in a angle element $\mathrm{d}\theta_r$, and with the relation:

$$\mathrm{d}\theta_{\mathrm{r}} = \frac{n_{\mathrm{Si}}}{n_{\mathrm{air}}} \cdot \frac{1}{\cos\theta_r} \cdot \mathrm{d}\theta_0. \tag{2.20}$$

If the transmittance of the emitted light through the SiO_2 layer is termed as T, then the light intensity within a solid angle element in the silicon substrate, $\mathrm{d}\Omega_{\mathrm{Si}}$, will relate to that within a solid angle element in air, $\mathrm{d}\Omega_{\mathrm{air}}$, by the expression

$$I_{\mathrm{air}}(\lambda) \cdot \mathrm{d}\Omega_{\mathrm{air}} = I_{\mathrm{Si}}(\lambda) \cdot T(\theta_0, \lambda) \cdot \mathrm{d}\Omega_{\mathrm{Si}}. \tag{2.21}$$

Note that the transmittance is a function of incident angle θ_0 and wavelength, T(θ_0, λ). In spherical coordinate system, for the solid angles one has

$$\mathrm{d}\Omega_{\mathrm{air}} = \sin\theta_r \cdot \mathrm{d}\phi\,\mathrm{d}\theta_r; \qquad \mathrm{d}\Omega_{\mathrm{Si}} = \sin\theta_0 \cdot \mathrm{d}\phi\,\mathrm{d}\theta_0 \cong \theta_0\,\mathrm{d}\phi\,\mathrm{d}\theta_0 \tag{2.22}$$

with $\mathrm{d}\phi$ is the angle element of the azimuth-angle, ϕ , and $0 < \phi < 2\pi$.

Replace (2.20) and (2.22) into (2.21) we obtain the *Lambertian* emission pattern which is expressed as

$$I_{\mathrm{air}}(\lambda) = I_{\mathrm{Si}}(\lambda) \cdot T(\theta_0, \lambda) \left(\frac{n_{\mathrm{air}}}{n_{\mathrm{Si}}}\right)^2 \cos\theta_{\mathrm{r}}. \tag{2.23}$$

where I is the radiant intensity which is expressed in power per unit of solid angle (W sr^{-1}).

This shows that the light intensity distributes in air according to the Lambertian emission pattern. The schematic Lambertian emission pattern is shown in Figure 2.7.

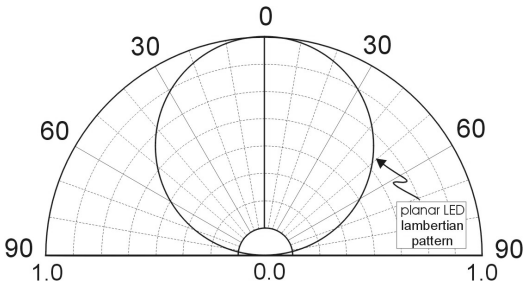


Figure 2.7: Lambertian emission pattern from a planar LED.

Now we consider a point light source generating photons with wavelength λ in silicon with the total source power of $\mathrm{P}_{\mathrm{source}}(\lambda)$. Assuming that the light distributes equally in all directions (independent on θ_0), thus the light intensity at a distance *r* from the source in silicon is determined by the ratio of $\mathrm{P}_{\mathrm{source}}(\lambda)$ and the spherical-surface area, $I_{\mathrm{Si}}(\lambda) = \frac{P_{\mathrm{source}}(\lambda)}{4\pi r^2}$. And the total light power emitted in the air $P_{\mathrm{air}}(\lambda)$ can be extracted by taking the integration of the intensity $I_{\mathrm{air}}(\lambda)$ over the entire hemisphere (radius *r*) on top of the light-source surface [21]. Thus we can express the relation of the light power inside and outside the device as

$$P_{\mathrm{air}}(\lambda) = \int_{\theta_r=0}^{\frac{\pi}{2}} \frac{P_{\mathrm{source}}(\lambda)}{4\pi r^2} T(\theta_0, \lambda) \left(\frac{n_{\mathrm{air}}}{n_{\mathrm{Si}}}\right)^2 \cos\theta_r \cdot (2\pi r \sin\theta_r)(r\mathrm{d}\theta_r). \tag{2.24}$$

From this expression we are able to extract the relationship (extraction coefficient, $C(\lambda)$) between internal and external efficiency of the light source at wavelength λ from the equation

$$C(\lambda) = \frac{P_{\mathrm{air}}(\lambda)}{P_{\mathrm{source}}(\lambda)} = \frac{1}{4} \left(\frac{n_{\mathrm{air}}}{n_{\mathrm{Si}}}\right)^2 \int_{\theta_r=0}^{\frac{\pi}{2}} T(\theta_0, \lambda) \cdot \sin(2\theta_r) \cdot \mathrm{d}\theta_r. \tag{2.25}$$

Note that the transmittance $T(\theta_0, \lambda)$ in the Eq. (2.25) also depends on the transmittance angle θ_r because it depends on the incident angle θ_0, while θ_0 is

related to the transmittance angle θ_r as mentioned in Eq. (2.19). So now in order to calculate the extraction-coefficient for our fabricated light-sources, we just need to extract the transmittance T(θ_0, λ) for each corresponding light-source structure, and then replace it into Eq. (2.25). From the obtained value of T(θ_0, λ), if defining the mean transmittance of the light source for all emitted light within the escape cone as $\bar{T}(\lambda)$, we can bring $\bar{T}(\lambda)$ out of the integration in the equation (2.25) then we have

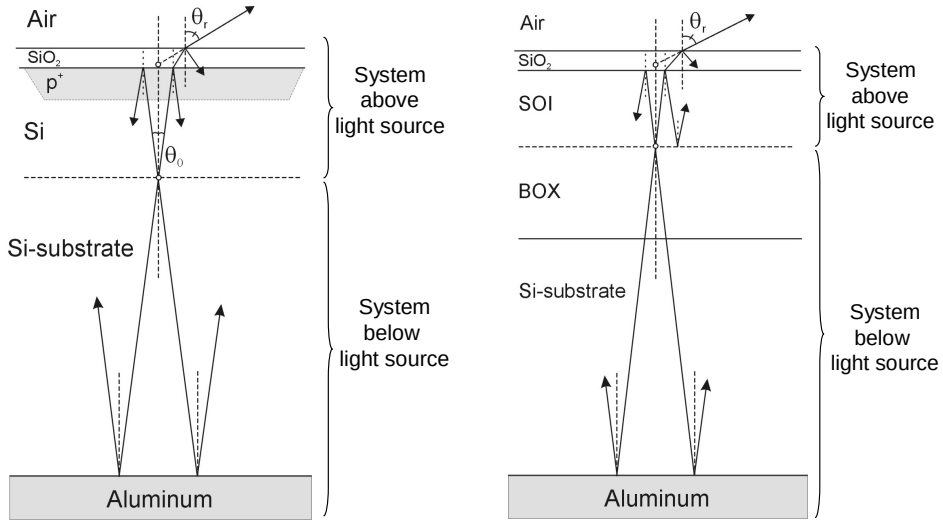
$$C(\lambda) = \frac{1}{4}\left(\frac{n_{\text{air}}}{n_{\text{Si}}}\right)^2 \bar{T}(\lambda) \int_{\theta_r=0}^{\frac{\pi}{2}} \sin(2\theta_r) \cdot \mathrm{d}\theta_r$$
$$\Rightarrow C(\lambda) = \frac{1}{4}\left(\frac{n_{\text{air}}}{n_{\text{Si}}}\right)^2 \bar{T}(\lambda). \tag{2.26}$$

In the following sections we will present how the transmittances of the realized light sources are calculated.

2.2.4 Transmittance of the emitted light from bulk-Si LEDs and SOI LEDs

Since photons can be generated at any position (where electrons and holes can probably travel to) within the silicon layer, the model will not be specified if we just analyze a point-like light source at a certain position within the silicon layer. That point light source generates light equally in all directions (i.e., the symmetrical light source). In order to calculate the total transmittance of the emitted light for the realized light sources, we divide the light source into two separate systems: the first one includes all layers above the light source, and the second system includes all layers below the light source (see Figure 2.8).

For the light reflected from the backside we can treat it according to two options: 1) we assume the backside to be perfectly flat; 2) we assume the backside to be rough. In the first case all the light outside the critical cone will be reflected geometrically and is in this way waveguided to the edge of the wafer, meanwhile suffering from absorption. The light inside the escape cone and directed both upwards and downwards will eventually be emitted at the front-side when we assume 100 % reflection for the Al or it will partly be absorbed. In the second case all the light reaching the backside, which includes also the light outside the escape cone after being reflected by the front-interface, will be diffusively reflected and may reach the frontside again but for the greater part it will reach the frontside outside the critical angle and reflect back. It can be argued that the total amount of light emitted at the front side is larger in the case of a rough backside. It will, however, be diluted strongly and due to the 500 μm wafer thickness be emitted over a very



(a) Model for bulk LED (b) Model for SOI-LED

Figure 2.8: Calculation model used for: (a) bulk Si LEDs; (b) SOI LEDs.

large area outside the reach of our detector or below the detection limit. For a rigorous calculation of the light emitted at the frontside, information on the backside roughness and the wavelength dependent aluminum reflection is required. Poor knowledge on this made us decide to calculate for the cases where the backside reflection was or was not taken into consideration. In particular for SOI devices, the device dimensions are very small compared to the wafer thickness and therefore any backside reflection should be visible outside the device. The intensity of light outside the device area was, however, below the detection limit of our detection system. And as a result, in that case while only integrating the light inside the device area the assumption of ignoring the backside reflection is valid. Thus in our calculation of the transmission for SOI LEDs we just consider for the case of no backside reflection.

In the case of bulk silicon LEDs in our experiments, the highly doped p^+ region was realized at $\sim$1 μm depth below the Si/SiO_2 interface. As a 100 mA forward current flows through the LEDs, carriers can diffuse deeply into the silicon substrate. The diffusion length can be calculated easily for holes at that working condition, and it shows that the main path of the recombination takes place within $\sim$100 μm silicon counting from the p^+/n junction. Based on these realities, in our calculation model for a bulk Si-LED, we chose the first thin-film system above the light source to include 100 μm lowly-doped Si/1 μm highly-doped silicon/20 nm SiO_2/air; and the second system below the light source including 400 μm lowly-doped Si/1 μm Al/air (see Figure 2.8a).

For the SOI LEDs, the first thin-film system above the light source was chosen with 150 nm lowly-doped Si/20 nm SiO_2/air; and the second system was 400 nm SiO_2/500 μm lowly-doped Si/1 μm Al/air (see Figure 2.8b). In our SOI LEDs, the same as in bulk Si LEDs, the backside Si/Al interface was formed without polishing (not flat).

The reflectance (the fraction of energy reflected) and the transmittance (the fraction of energy transmitted) for the thin-film system above the light-source are termed R_1 and T_1, respectively. Similar for the system below the light-source, its reflectance and transmittance are R_2 and T_2, respectively. These parameters were calculated by using the Eq. (2.17) and (2.18). We assume that the generated light is non-polarized light. Thus all the obtained parameters of R_1, T_1, R_2, T_2 were extracted as the mean value of the two linearly s-polarized (transverse electric TE) and p-polarized (transverse magnetic TH) parts. The total transmittance for the complete system (including two thin-film systems) will be the sum of three components, which can be expressed as

$$T(\lambda, \theta_0) = \frac{1}{2}\,(T_1 + T_{\mathrm{r1-r2-t}} + T_{\mathrm{r2-t}}) \tag{2.27}$$

where the first component T_1 denotes the direct transmission part from the light-source through the first system; the term $T_{\mathrm{r1-r2-t}}$ signifies the second component which was transmitted through the top system after being reflected from the first system and then the second system respectively; and the term $T_{\mathrm{r2-t}}$ presents for the transmittance component which was firstly reflected upward by the second system and then emitted to air through the first system.

If we take the multiple reflections at the interface between these two systems into account we have to add up all the transmitted parts after each reflection. Now we calculate each component in the equation (2.27). The total amplitude of the successive transmitted light is calculated as

$$\begin{aligned} T_{\mathrm{r1-r2-t}} &= R_1\,R_2\,T_1 + R_1\,R_2\,(R_1\,R_2)T_1 + R_1\,R_2(R_1\,R_2)^2T_1 + \ldots \\ &= R_1\,R_2\,T_1 + (R_1\,R_2)^2T_1 + (R_1\,R_2)^3T_1 + \ldots \\ \text{Then}\quad T_1 + T_{\mathrm{r1-r2-t}} &= T_1\,\left[1 + (R_1\,R_2) + (R_1\,R_2)^2 + \ldots\right] \\ &= T_1\,\frac{1}{1 - R_1\,R_2}. \end{aligned} \tag{2.28}$$

In this expression we used the aid of the series expansion

$$\frac{1}{1-x} = 1 + x + x^2 + \ldots$$

Similar for the third component $T_{\mathrm{r2-t}}$, we can have

$$\begin{aligned} T_{\mathrm{r2-t}} &= R_2\,T_1 + R_2(R_1\,R_2)T_1 + R_2(R_1\,R_2)^2T_1 + \ldots \\ &= R_2\,T_1\left[1 + (R_1\,R_2) + (R_1\,R_2)^2 + \ldots\right] \\ &= R_2\,T_1\frac{1}{1 - R_1\,R_2}. \end{aligned} \tag{2.29}$$

Thus the total transmittance of all three components now is given by:

$$T(\lambda, \theta_0) = \frac{1}{2}\,\frac{(1 + R_2)}{1 - R_1\,R_2}\,T_1. \tag{2.30}$$

In the next sections the results of the calculations are presented.

For bulk silicon LEDs

If the reflection from the backside of the silicon wafer is not taken into consideration, the transmittance part of the emitted light is just calculated for the light generated within 100 μm thick silicon volume counting from the Si/SiO_2 interface. The transmittance as a function of wavelength for the case when the light is

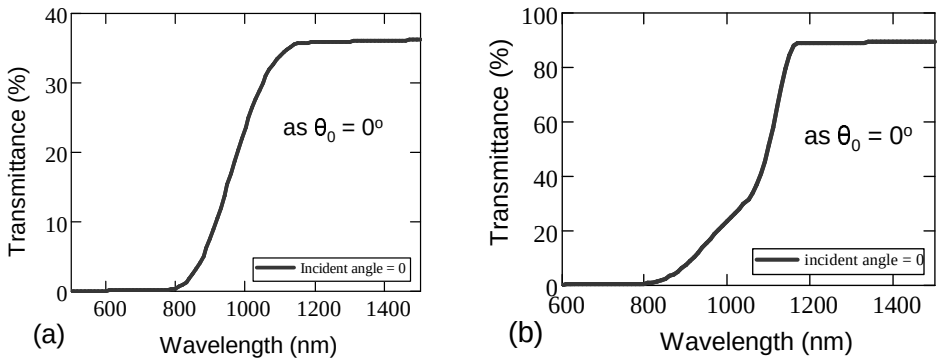


Figure 2.9: Transmittance of light for our bulk LEDs as a function of wavelength when the light-ray is perpendicular to the interface: (a) backside reflection ignored; (b) back-reflection taken into account.

perpendicular to the interface ($\theta_0 = 0$) is shown in Figure 2.9a. We can see that cut-off wavelength of the transmission is about 800 nm.At the wavelength of the silicon band-edge ($\sim$ 1150 nm), the transmittance is just 37 %. This low level of transmittance can be explained by the re-absorption of the silicon volume above the light-source and by the reflection at the Si/SiO_2 interfaces.

If the backside reflection is taken into consideration (see in Figure 2.9b), the transmittance is strongly enhanced, which is 88 % at the wavelength of 1150 nm.

We see that this high level of the total transmittance is lager than two times of the previously extracted transmittance ($> 2 \times 37$ %). This is because the light part with $\lambda > 1150$ nm, which was reflected back from the Si/SiO_2 interfaces above the light source, after traveling through the thick silicon substrate (with almost no absorption) is again reflected upward by the Si/Al interface.

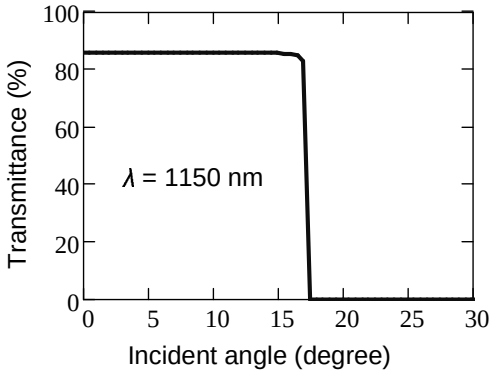


Figure 2.10: Total transmittance of emitted light out of bulk LEDs as a function of incident angle at wavelength of 1150 nm.

As mentioned in the previous sections, the transmittance of emitted light also depends on the incident angle of the light-ray, θ_0. At the silicon band-edge emission ($\sim$ 1150 nm), this dependence for the case as the backside reflection was taken into account is presented in Figure 2.10. We can see that all the light outside the cone with the apex angle of $\sim 33^\circ$ ($2 \times \theta_{\mathrm{crit}}$) will be totally reflected back and the transmittance is almost constant for the light inside this cone.

Then we can take the mean value of the transmittance to extract the extraction-coefficient for bulk Si LEDs at λ = 1150 nm using Eq. (2.26). The values are 0.0176 and 0.0074 for the case with and without backside reflection respectively. Or in other words, in order to obtain the internal efficiency of bulk Si LEDs we need to multiply the external efficiency by 57 when counting also the backside reflection or by 135 when ignoring the part reflected from the backside.

For SOI LEDs

In fact for SOI devices, the light generated within the 150 nm SOI layer if propagating downward, in order to reach the top layer again it has to be in two times passing through the BOX layer and the 500 μm thick substrate. Therefore, the light reflected from the backside Si/Al interface just contributes a small fraction to the total transmittance of the SOI devices. Thus in the next calculation of the transmittance for our SOI LEDs, we only consider the case of no backside reflection.

When the backside-reflection is ignored, the transmittance part of the emitted light is just calculated for the light generated within the volume of the 150 nm thick SOI thin-film. The total transmittance includes the direct transmitted part and the parts reflected back from the Si/BOX interface and the BOX/substrate interface.

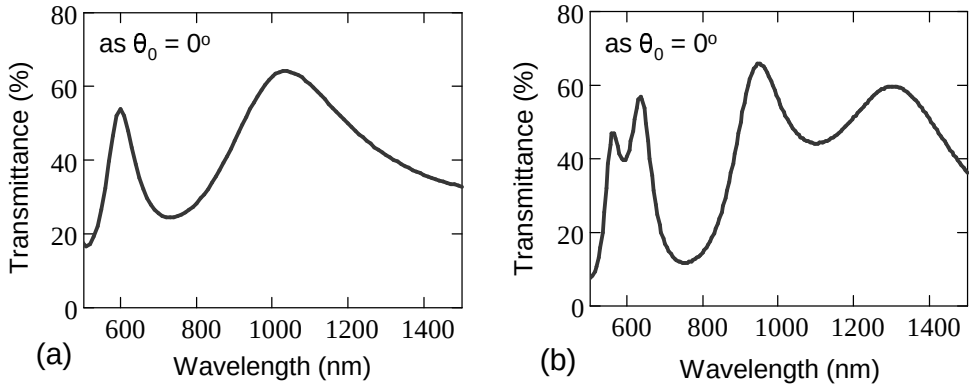


Figure 2.11: Transmittance of light in our SOI LED structures as a function of wavelength when the light-ray is perpendicular to the interface: (a) interference from the BOX layer ignored; (b) both interferences happening in the SOI and BOX layer taken into account.

Note that, the peaks in Figure 2.11 correspond to the condition of the constructive interference occurs in the thin films when the optical thickness equals an integer number of half a wavelength or $n\,d = \frac{1}{2}\mathrm{m}\lambda$. In order to investigate separately the influence of interference occurring in the BOX layer on the transmittance of our SOI-LED structures, we do calculations for two conditions as the interference occurring in the BOX layer was or was not taken into consideration (see Figure 2.11).

The total transmittance from SOI LEDs as a function of wavelength for the light perpendicular to the interface ($\theta_0 = 0$) is shown in Figure 2.11. We can clearly see that the interference of the emitted light occurred within the SOI layer from Figure 2.11a, whereas from Figure 2.11b the combination of both interferences happening in the SOI and BOX layer can be observed. It shows that the interference happening in the BOX modified the positions (the wavelength) of the transmittance peaks.

The incident angle dependence of the total transmittance (including the reflection from Si/BOX and BOX/substrate interfaces) for SOI LEDs was calculated for the wavelength of 950 nm and 1150 nm. This is exhibited in Figure 2.12. We see that the escape cone is a little bit different for different wavelengths and at the same magnitude level with bulk Si LEDs. The transmittance varied from 46 % to

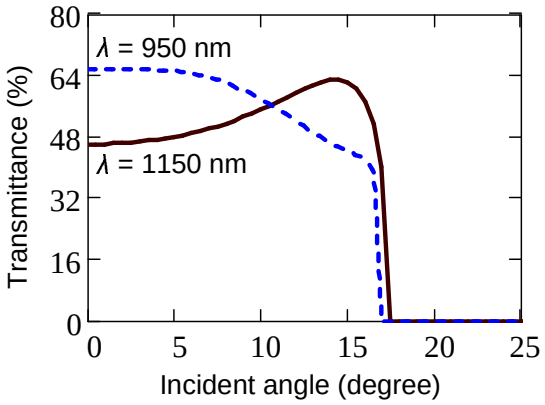


Figure 2.12: Total transmittance of emitted light out of SOI LEDs as a function of incident angle for 950 nm and 1150 nm wavelength.

66 % depending on the incident angle. Thus in order to calculate the extraction coefficient for SOI LEDs we take a mean value of the total transmittance of 56 % and using the Eq. (2.26) we have C = 0.0112. It also means that to extract the internal efficiency of SOI LEDs we need to multiply the external efficiency by a factor of 89.

From these calculated data, we can see a large influence of the re-absorption of silicon wafer on the total transmittance, special for bulk LEDs. This suggests that the externally observed emission spectrum of the LEDs would also be affected by the re-absorption. This influence was carried out and will be presented in the next section.

2.2.5 Calculation of emission spectra from bulk and SOI LEDs

In 1982, Würfel extended the thermal radiation theory of Planck for many different kinds of radiation [22]. In that theory, the excitation states of a semiconductor is characterized by their chemical potential: μ_{c} and μ_{v} is the chemical potential of a single state at the conduction-band and at the valence-band, respectively. Under the equilibrium condition between the excitations of a semiconductor, the chemical potential of photons is defined as $\mu_\gamma = \mu_{\mathrm{c}} - \mu_{\mathrm{v}}$. From the general radiation equation, the generalized Kirchhoff law was introduced for the photon current, $\mathrm{j}_\gamma(\mathrm{h}\,\nu, \mu_\gamma)$, emitted from an emitter

$$\mathrm{j}_\gamma(\mathrm{h}\nu, \mu_\gamma) = \alpha(\mathrm{h}\nu)\frac{8\pi^2(\mathrm{h}\nu)^2}{\mathrm{h}^3\,\mathrm{c}^3}\left[\exp\left(\frac{\mathrm{h}\nu - \mu_\gamma}{\mathrm{k\,T}}\right) - 1\right]^{-1} \tag{2.31}$$

with $\mathrm{h}\nu$ is photon energy; $\alpha(\mathrm{h}\nu)$ is the absorption coefficient of the semiconductor; c is the light velocity in vacuum; and $k\,T$ is thermal energy.

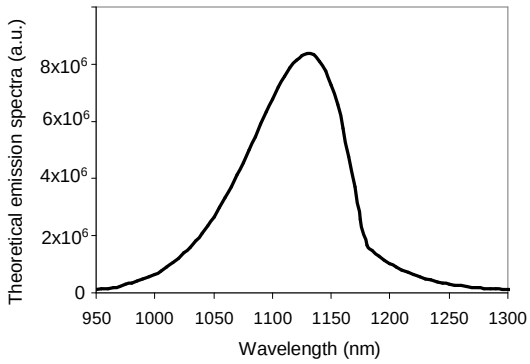


Figure 2.13: Theoretical spectra calculated for Si LEDs at 300 K.

Thus, the spectrum of luminescence intensity of a light emitting device can be calculated theoretically. By using the calculated data of the Si absorption coefficient (previously presented in Figure 2.5) and by combining it with Eq. (2.31) we can derive the theoretical emission spectrum for a Si LED. An example of the calculated emission spectrum of the Si LED at 300 K is shown in Figure 2.13.

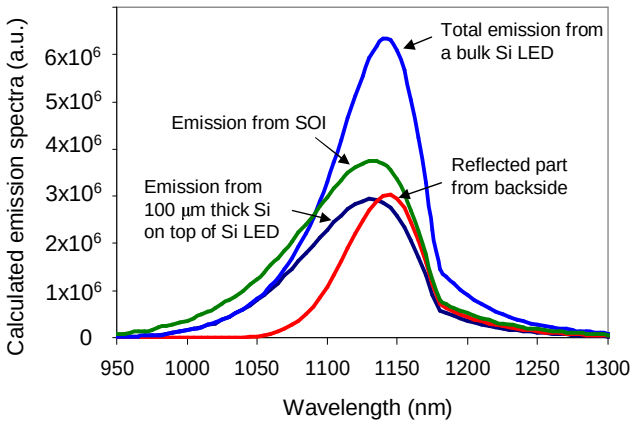


Figure 2.14: Comparison of theoretical spectra from bulk Si and SOI-LEDs. The spectrum of SOI LED was calculated for the case with the interference in both SOI and BOX layer (Figure 2.11b) but no backside reflection taken into consideration.

The product of the photon currents, $\mathrm{j}_\gamma(\mathrm{h}\nu)$, and the transmittance of the Si LEDs, $T(\mathrm{h}\nu)$, will result in the emission spectrum of the Si LEDs. Now in order to analyze the re-absorption effects of Si on the emission spectrum for different structures (bulk and SOI), we used our calculations of the transmittance for these structures.

The emission spectra from bulk Si LEDs at 300 K for the case with and without backside reflection are presented in Figure 2.14. We see that the emission

peak shifts to the longer wavelength when the backside reflection is taken into account. This is because in that condition the light with a shorter wavelength was re-absorbed stronger by the large volume of the silicon substrate.

For SOI LEDs, since the light is generated mostly in the SOI layer, the emission peak shifts to the shorter wavelength. We use the transmittance shown in Figure 2.11b to calculate the spectrum from SOI LED, and this also can be seen in Figure 2.14.

Conclusion

Based on the main possible recombination processes occurring in a silicon LED, the internal quantum efficiency of the luminescence processes (EL and PL) was calculated for a range of excess carrier concentration from 10^{15} to 10^{19} /cm^3. The calculated data show that at low injection condition, when the SRH recombination is the dominant process, the impurity level (deep level impurities) is the most important parameter in both cases of bulk-silicon LEDs or SOI LEDs, which controls the fraction of the competing radiative band-to-band recombination rate to the total rate of all other non-radiative recombination processes. However, at a higher injection level the device efficiency is controlled by the Auger recombination process. For the light emitting devices realized on SOI material, the non-radiative recombination at the interface and junctions is a key issue related to the device efficiency. To improve the light emitting efficiency, the non-radiative processes must be suppressed sufficiently. This can be done by limiting the contamination level during device fabrication processes, by improving the Si/SiO_2 interface quality, and by introducing a potential barrier to block electrons and holes from reaching the p^+/n^+contacts.

According to the theory of optics and reported experimental data, a model was introduced to investigate quantitatively the relation between external and internal efficiency of a light source. The relationship between internal and external efficiency of our realized light emitting devices was given by extraction from the built models. The influence of the backside reflection on the transmittance coefficient and the emission spectrum of the light sources realized on bulk silicon wafers is stronger compared to that of the light sources realized on SOI material.

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Chapter 3

Optical Measurement Equipment and Calibration

Abstract

The electrical and optical analysis equipment used in this work is reviewed in the first part of this chapter. Short descriptions of each optical instrument are presented. Calibration of the optical system is an important issue to confirm the reliability of the obtained results. In the second part, all information about the equipment used and procedures carried out in the calibration process of the optical system are described.

3.1 Electrical Characterization Equipment

Electrical measurements, including I-V and C-V characterizations, are all carried out on a Cascade and Karl Suss PM8 probe station and with an Agilent 4156C parameter analyzer.

3.2 Optic Analysis Equipment

All optical analyses performed in this work were made on two measurement systems. In the first system, emitted light is collected by an optical probe (Lightwave Probe or LWP), and then the collected signals are guided to a scanning spectrometer (Spectro 320) by an infrared optical fiber. In the second system, light emitted from the object is collected by a microscope and imaged on a calibrated infrared camera (XEVA Camera), where the images are processed to the desired data by suitable software.

More detailed descriptions of these two systems are presented as follows.

3.2.1 Fiber Optic Probe System

The fiber optic probe system includes the optical probe, fiber cable, and spectrometer. A drawing of position of the optical probe and device on the chuck during measurements is shown in Figure 3.1.

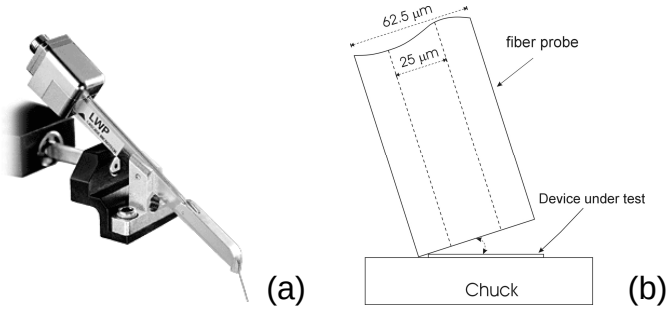

Figure 3.1: (a) A photo of the LWP Lightwave probe [1]; (b) Drawing of relative position between fiber-probe and device under test.

Probe: The optical probe used here is the LWP Lightwave probe. This probe (see Figure 3.1) is optimized for use with the Cascade Microtech probe station and is convenient for optical characterization in combination with electrical measurements. The LWP Lightwave probe includes an infrared optical fiber mounted

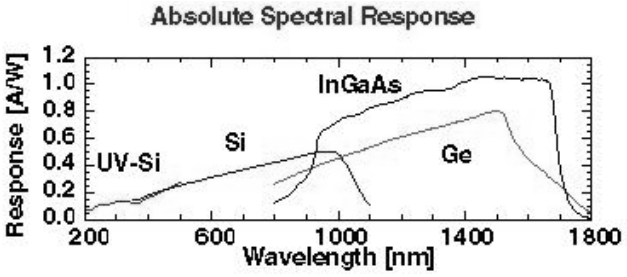

Figure 3.2: Spectral response of Si, InGaAs and Ge detector as a function of wavelength (A/W = Ampere of sensor output per Watt of incident light power) [2].

into a holder, which is designed not only to stabilize the fiber-probe on the probe-station but also to enable the probe to change the light collecting angle of the fiber. The used optical fiber is a lensed-multimode fiber with core and outer diameters of 25 and 62.5 μm respectively.

Fiber-Optic Cable: The optical cable is used to transfer the collected signals from the Lightwave probe to the spectrometer. The infrared fiber used is of the step-index type with a core numerical aperture of 0.22 ± 0.02 and two ends fitted with standard SMA connectors.

Spectrometer: The transferred signal is processed by the Spectro 320. The Spectro 320 has a focal length of 320 mm and it includes two detectors: a silicon detector and an InGaAs (infrared) detector. Therefore, it is sensitive for a wavelength range from 190 nm to 1700 nm and suitable for analysis of our fabricated silicon-based light emitting devices. Typical spectral response curves of InGaAs, Germanium and Silicon detectors are shown in Figure 3.2.

3.2.2 Microscope and Camera System

A schematic overview of the system is shown in Figure 3.3. The infrared light emitted from the device under study is collected by an objective lens and then passes through all the optical elements of the microscope. A splitter in the optical break-out box splits the light beam: 30-40 % of the light goes to a panchromatic camera for a top-view image of the device-structure; the remaining part transmits to the XEVA camera. The Specim spectroscope for signal analyzing can be installed optionally.

Now let's go to the detailed parameters of each component of the system.

Infrared Camera. We use an infrared XenICs (XEVA) USB camera, which combines a thermo-electrically cooled detector head with the control and communication electronics. The camera head is designed to fit within an aluminum anodized housing. A standard C-mount lens is mounted on the housing. A suit-

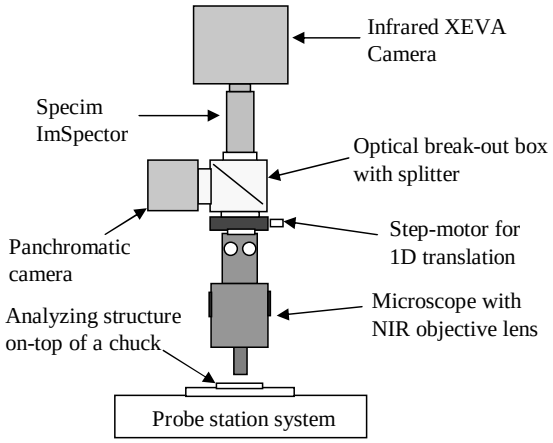

Figure 3.3: Schematic overview of the microscope-camera system.

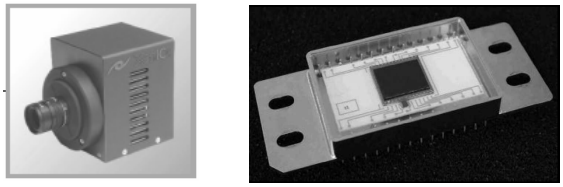

Figure 3.4: *(left)* The XenICs camera; *(right)* Picture of the 2D array of InGaAs photodiodes (XFPA-1.7-320-TE1 detector) [3].

able adapter can be used to connect the camera either directly to the microscope system or via a Specim ImSpector.

The detector used in the XEVA camera is the XFPA-1.7-320-TE1, a matrix of (256×320) InGaAs photodiodes (on the right of Figure 3.4). InGaAs diodes are specifically suited for near-infrared (0.9 - 1.7 μm) imaging. A typical photoresponse of the XenICs InGaAs is presented in Figure 3.5. A temperature controller is used to regulate the thermo-electric cooler for stabilization of the detector working temperature. A chiller is used to provide water into the inlet-pipe at the rear end of the camera for cooling the thermo-electric cooler. An analogue-to-digital converter is used to translate the pixel information into the desired form.

Specim ImSpector. A combination of the XEVA camera and an Imspector creates a spectral imaging device. captures a line from the image through a slit and disperses the light from this line to a spectrum. The spectral image contains spatial information in one axis and spectral information in the other axis. As a result, it is possible to acquire full-spectral information from each line image captured from the target. Then a 2-D spectral image can be formed if the ImSpector sequentially

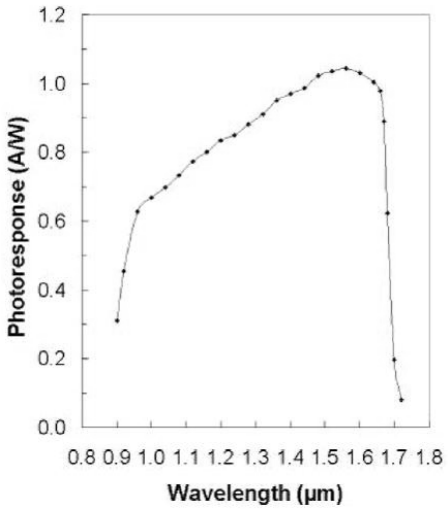

Figure 3.5: Typical photo-response of the XenICs infrared camera as a function of wavelength [3].

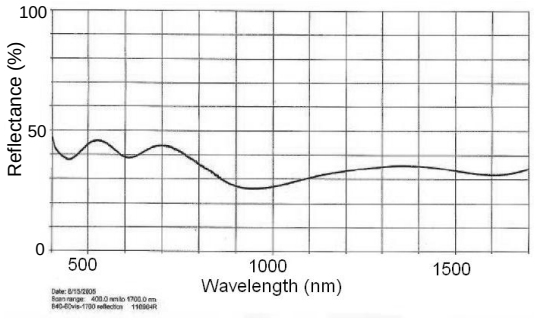

Figure 3.6: The reflectance of the splitter as a function of wavelength [3].

captures images from the target by either moving itself or moving the target in a way that the slit can scan through the target-surface. In our case, in order to have the image of the device under study, we use a step-motor to move the ImSpector.

Splitter. About 60-70 % of the light incident on the break-out box enters the ImSpector/camera. The other fraction is reflected to a panchromatic camera, which is used just for viewing the device under test. From Figure 3.6 it can be seen that the transmittance, which is (1 - reflectance) of the splitter slightly decreases in the range of 950 nm to 1350 nm (the wavelength range of interest for Silicon LEDs).

Step-motor. It is designed as an adapter connecting the spectroscope to the camera-ImSpector system. The motor does the 1-D movement and subsequently brings the system staying on-top of it to a new position along to the translation

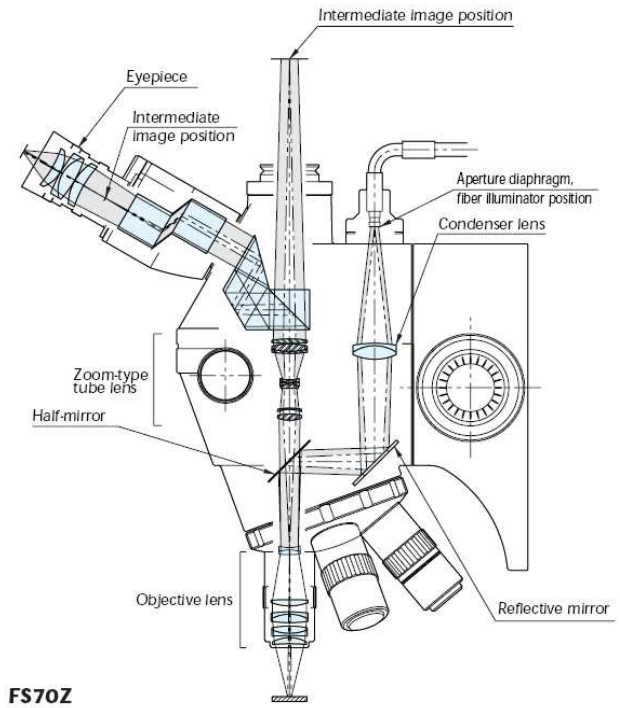

Figure 3.7: A schematic structure of the microscope Mitutoyo FS70Z unit [4].

direction. The step-size of each movement step is 30 μm; and the moving speed of the camera can be controlled by software (X-Cube). Each spectral line image of the target is stored by the ImSpector after each movement-step of the step-motor. In this way the hyperspectral image of the whole emitting area can be recorded.

Microscope. The microscope system used in our laboratory is the Mitutoyo FS70Z model. The schematics of this system is shown in Figure 3.7. In our experiments we used objective lenses with magnification ranging from 5x to 50x. However, the calibrated experiments were performed only with M Plan Apo(chromat) near-infrared (NIR) lenses for 10x, 20x and 50x magnification. The specifications of these lenses are shown below in Table 3.1. Typical transmission characteristics of M Plan Apo lenses are shown in Figure 3.8. For NIR lenses, it shows that transmission decreases when wavelength increases from 900 to 1500 nm. As a result, the losses due to absorption of the microscope system would increase with wavelength in the NIR range.

It should be kept in mind that the other optical components in the microscope system, as shown in Figure 3.7, such as beam-splitters and additional lenses are not optimized for transmission in the NIR range. Thus the losses because of these components can be large.

Software. Control of the XEVA camera for each set-up configuration (stand

Model & Magnification	N.A. Numerical aperture	W.D. [mm] Working distance	f [mm] Focal length	R [μm] Resolving power	$\pm$ D.F. [μm] Depth of focus
M Plan Apo NIR-10x	0.26	30.5	20	1.1	4.1
M Plan Apo NIR-20x	0.40	20	10	0.7	1.7
M Plan Apo NIR-50x	0.42	17.0	4	0.7	1.6

Table 3.1: Specific information of the infrared objective lenses [4]

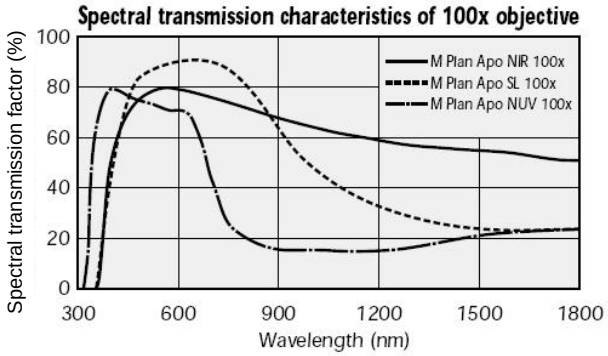

Figure 3.8: Spectral transmission characteristics of 100x objective lens [4]: NIR = Near-infrared; SL = Super-long (working distance); NUV = Near-ultraviolet.

alone or combined with ImSpector) is performed by means of the X-Control or X-Cube software.

3.2.3 Calibration of the microscope system

Equipment used for calibration

Firstly, we describe all characteristics of the equipment used in the calibration process.

Pencil Light Source. The pencil lamp used in our wavelength calibration is a 6030 Argon (Ar) lamp with the output spectrum shown in Figure 3.9 and the used wavelength peaks (in infrared-range) is presented in Table 3.2.

Light source. A 150 W Quartz Tungsten Halogen lamp with a broad emitting spectrum (see Figure 3.10) is used as a light source for the calibration process.

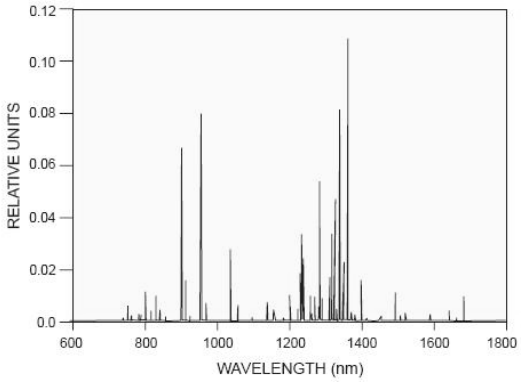

Figure 3.9: Output spectrum of 6030 Argon lamp, run at 10 mA [5].

Peak number	1	2	3	4	5	6	7
Wavelength (nm)	912.3	922.4	965.8	1047.1	1331.3	1336.7	1371.8

Table 3.2: Useable peak wavelength of Ar lamp in the infrared range [5].

Optical fiber. To guide the light from the light source to the microscope, a glass randomized bundles fiber cable is used. This fiber was chosen because it gives a good uniform output and it can withstand up to 180 °C. The transmission characteristics of this fiber are shown in Figure 3.11. A liquid infrared fiber showed a higher transmittance compared to the glass bundles fiber but it appeared to be unstable due to the heat absorbed from the light source, which changed its transmittance during measurement.

Filters. A filter-wheel is installed between the light-source and the optical fiber. A set of filters: 400 nm; 600 nm; 800 nm; 1000 nm; 1200 nm; G850; G1000; and a heat absorbing filter was installed into this filter-wheel. Since the spectral range of our fabricated silicon LEDs is from 850 nm to 1350 nm, we just used for calibration the 1000 and 1200 nm wavelength filter. For a rough overall calibration, we also used two broad bandpass filters: the G850 and the G100 for the transmission in the range of 850-2800 nm and 1000-2800 nm, respectively.

Radiant power/energy meter (Figure 3.12). This measures radiant power and energy directly (i.e., no more scale/calibration factors are needed) with a flat response ($\pm$ 1.5 %) independent of wavelength for the UV - IR in the readout power range from 100 pW to 3 W.

Silicon diode detector. This covers the range from 220 nm to 1100 nm. The spectral response characteristics of the silicon detector are shown in Figure 3.2. A snap-on attenuating filter can be used to extend the maximum power range from 1-3 mW to 100-300 mW. The detector is actually a 10 $\times$ 10 mm^2 silicon probe.

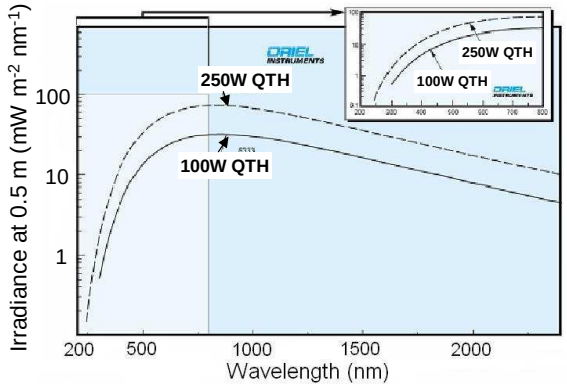

Figure 3.10: Typical spectral irradiance of 250 W and 100 W Quartz Tungsten Halogen lamp [5].

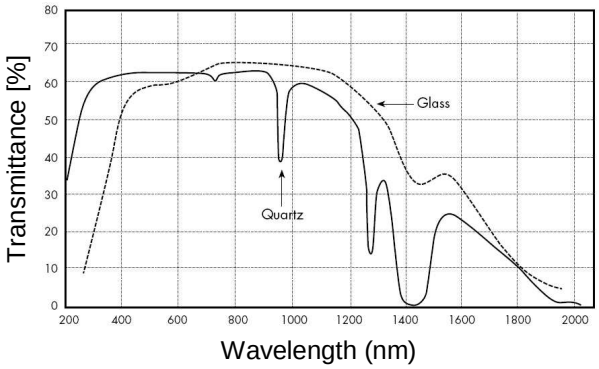

Figure 3.11: Typical transmittance of bundles fibers. The dash line indicates transmittance of glass bundles fiber used in our calibration [5].

This probe is used to calibrate the visible camera (not presented here in this book).

Germanium Probe. This is a near infrared probe including a 5×5 mm^2 Germanium detector. It detects signals in a wavelength range of 800-1600 nm. Without attenuating filter, it covers a power range of 1 nW-30 mW. With the filter fitted it can measure a maximum power up to 300 mW. Figure 3.2 presents also the spectral response of the Germanium detector.

Labsphere diffuse reflector. It is termed as Spectralon (see Figure 3.13), a commercially available diffuse reflectance material made from polytetrafluoroethylene (PTFE). The Spectralon CSRT-99-020 material is the most Lambertian reflector available for use over the wavelength range from 250 nm to 2500 nm. In the wavelength range of 850-1500 nm the Spectralon has a (diffuse) reflection coefficient of 99.8 %.

Figure 3.12: Radiant power/energy meter with a probe [5].

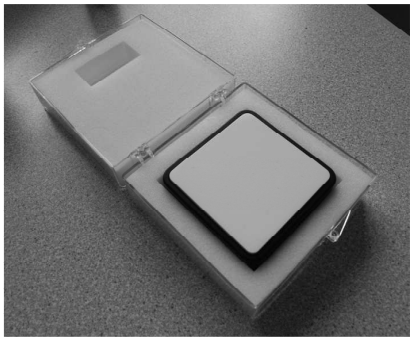

Figure 3.13: A photo of the Labsphere diffuse reflector (Spectralon).

Calibration procedures

Next all steps of the calibration process are discussed.

The *first step* is the wavelength calibration of the infrared camera. Doing wavelength calibration of the camera means that we need to calibrate the spectral axis of a spectral image to a known position in the pixel-matrix of the camera. Therefore, the camera and the ImSpector should be aligned in such a way that the spatial axis of the spectrograph is parallel to the horizontal pixel lines of the camera. The alignment procedure is described in the camera manual.

In the spectral image of the pencil Ar lamp, seven horizontal bright lines corresponding to seven peak wavelengths in the infrared range of the Ar lamp can be clearly identified. These peak wavelengths are mentioned in the Ar lamp characterization section. Note that those spectral lines should be sharp and as narrow as possible. This indicates that the Imspector is in good focus. Otherwise, we need to focus it again by following the camera manual.

The wavelength corresponding to each spectral line can be read by positioning the cursor on this line on the spectral image. At the same time, the corresponding coordinates in the image are also displayed on the status bar of the screen. The

seven read wavelength values must be exactly the same as the seven wavelength peaks of the Ar lamp. If this is not the case, open the wavelength calibration data (Excel file) stored in the computer and then correct it. The observed Y coordinates should now belong to the wavelength peaks of the Ar lamp. As a linear regression is calculated in this Excel file, all 256 new wavelength values belonging to 256 vertical pixels are shown. Copy all these 256 wavelengths to the wlc file (wlcalXeva.wlc) and then store it at the same previous location.

The *second step* is determinations of the loss-factor of the microscopy system using a broad-spectral light source. In preparation for this calibration step, we measure the spot size on the object when the microscope is in focus. The microscope has three objective lenses of NIR-10x, NIR-20x, and NIR-50x. It is possible to do this accurately by focusing on a wafer with photoresist and developing the wafer after sufficient exposure. The spot diameters corresponding to the magnification of 10x, 20x and 50x are 3.920, 1.600, and 0.693 mm respectively.

After preparation, we perform a preliminary rough calibration by using the broad band filters. It is a rough calibration because the spectra of the light source at the object plane could be different compared to that at the image plane (absorption and reflection within the microscope is not the same for wavelength range studied). So we simply assume the losses of the microscope are the same for the full near-infrared range under study. After that, we choose a desired objective lens of the microscope. And then, the optical cable is used to guide the light from the light source into the microscope (with the G850 and G1000 filters).

The light power density (in W/cm^2) of the light source at the object position can be measured by a Ge detector. The Ge detector measures photocurrents and translates them into power by using a calibration data stored in the equipment's microprocessor. This translation can, however, only be done when the wavelength causing the photocurrent is set. We use a broad spectrum source and thus can not make this conversion correctly. Since we measure at the object and at the image position with the same detector and since we later on take the ratio of these two values to extract the loss-factor, it is possible to use an arbitrary value for the wavelength setting. We use the 1150 nm wavelength for the Ge detector in this calibration step. Since at all three magnifications the spot diameter is always smaller than the detector dimension (for both Si and Ge detector), we can determine the light power density within the spot in W/cm^2 by taking the ratio of the light-power, measured in W by the detector, to the spot area. The measured light power density is termed P_1.

Next, replace the detector by the Spectralon . This material reflects $>$99 % of the incident light in a Lambertian way. When the microscope is in good focus on the Spectralon surface, part of the measured light power is diffusely reflected back through the microscope and imaged at the focal plan. At this position, the spot-size is in general larger than the detector size. Therefore, the spot-size can

be ignored as we calculate this light power density in W/cm^2. The light power density at this position (P_2) is compared to the previously measured light power density on the chuck (P_1) and it allows the loss-factor of the object-microscope system to be determined.

We now know both the light power falling on the Spectralon in W/cm^2 and the power falling on the image plane (W/cm^2). Since the reflection of the Spectralon is $\sim$100 %, we can calculate a "transfer" factor of the total microscope system which includes all numerical apertures, beam-splitters and absorption. The loss-factor (F_{loss}) can be extracted from the formula:

$$P_1 = P_2 \cdot F_{\mathrm{loss}} \cdot M_{\mathrm{opt}}^2 \tag{3.1}$$

with M_{opt} is the magnification of the microscope.

In this 'rough' measurement, we do not include the spectral influence of the light source, microscope system and the detector. To improve the accuracy of the calibration, it is necessary to repeat the entire sequence of the above mentioned steps, however, now using a well-defined small band filter in the light path. Then we know the transfer factor for this particular wavelength.

In the *third step*, the calibration-factor for a relative unit (Analog-to-Digital Unit - ADU) is determined. As replacing the detector by the camera at the focal image plane of the microscope, the diode matrix of the camera is exposed completely by the light reflected from the Spectralon. Then the integrated light intensity (in ADU-counts) is collected by the camera with a certain integration time. Thus, we convert the integrated light intensity into counts per unit time (counts/seconds). By dividing this intensity to the number of pixels (256×320) we are able to calculate the light intensity of each pixel (counts/pixel/seconds). Each pixel has a size of 30×30 μm^2, so now we can calculate the light power density $P_2^{'}$ at the focal image plane measured by the camera into counts/second/cm^2. Then we can express the relation as

$$P_2 = F_{\mathrm{c}}\, P_2^{'}. \tag{3.2}$$

with F_{c} is the calibration-factor measured in Joule/count. Now from Eq. (3.2) we can calibrate one count into energy (Joule). Thus we can do for the broad spectrum light source and for the specific wavelengths as well.

The *next step* is determining the loss-factor of the microscopy system with a small-band filter. The emitting wavelength-range of the Si-based LEDs is from 900 nm to 1300 nm, and in order to improve the accuracy of the calibration we chose two filters which allow transmission at 1001 nm and 1202 nm wavelength. The peak-transmission of the 1001 nm and 1202 nm filter is 48.91 % and 36.47 %, respectively, whereas their bandwidth at 50 % is 9.31 nm and 11.67 nm respectively.

According to the typical characteristics of each optical component of the microscope system presented above, we see that the transmittance of the light through the complete system decreases with increase of wavelength. This means that at each magnification level the total losses of the complete microscope system increase with wavelength.

The *final step* is the spectrum calibration. In the case of spectral measurements the real external spectral intensity could be obtained by correcting for each wavelength. As we observed there is a considerable difference between the loss-factors of the 1001 nm and 1202 nm small band filters. However, in practice we did not perform this correction meaning that all the presented spectra in this thesis are without such a correction.

Calibration data

The loss-factor (F_{loss}) as a function of magnification using the light source in combination with a broad- and with a small-band filter: It shows that the loss-

Magnification	10x	20x	50x
Loss-Factor (F_{loss}) with G850	186	250	210
Loss-Factor (F_{loss}) with G1000	269	381	317
Loss-Factor (F_{loss}) with 1001 nm light	181	241	197
Loss-Factor (F_{loss}) with 1202 nm light	266	355	260
Mean Loss-Factor for the 850-1350 nm range	224	298	228

Table 3.3: Measured loss-factor (F_{loss}).

factor is different for different magnifications. This is probably due to different materials used in the different lenses. We can also see that the total loss-factor rises with longer wavelength. The losses measured with the G1000 filter are larger than that measured with the G850 filter. The F_{loss} at 1202 nm wavelength is larger than that at 1001 nm wavelength. This can be explained by the lower transmission of the optical components (for the lens see e.g. Figure 3.8) for longer wavelength.

For practical applications when we want to determine the efficiency of our LEDs we can derive a mean loss-factor of the microscope in the wavelength range of interest for each magnification (as shown in Table 3.3). In our experimental data we used the mean loss-factor corresponding to each magnification.

The calibration-factor (F_c) used to convert a relative unit (count or ADU) to a absolute light power (Joule/second = watt) was calibrated with the well-defined narrow-band light filters (1001 nm and 1202 nm) and presented in Table 3.4.

From the data measured with the well defined narrow-band filters, a mean calibration-factor of 1.8 ($\pm$ 0.3) $\times$ 10^{-18} J/ADU was calculated and used in all

	NIR-10x	NIR-20x	NIR-50x
Calibration factor (F_c = J/ADU) for 1001 nm light	1.8×10^{-18}	1.8×10^{-18}	2.1×10^{-18}
Calibration factor (F_c = J/ADU) for 1202 nm light	1.5×10^{-18}	1.5×10^{-18}	1.9×10^{-18}

Table 3.4: Measured calibration factors F_c in J/ADU.

subsequent calculations of absolute light intensity presented in this thesis.

Conclusion

The typical characteristics of each optical element have been presented. The equipment used for the calibration of the microscope and camera system was calibrated and certified by the suppliers. The essential information concerning the carried out procedures has been illustrated and the measured calibration-factors are presented and were in the predicted range. The calibration can be considered as an approval for the quantitative reliability of our experimental data.

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Chapter 4

Bulk Silicon LEDs with dislocation loops

Abstract

In this chapter we report on the mechanism of formation of defects in silicon crystals due to ion implantation and on the feasibility of various defect engineering approaches for the improvement of light emission of silicon p^+/n diodes. Among the crystal damages caused by ion implantation, dislocation loops are effective in the carrier recombination process and influence the light emission mechanism when introduced close to the p^+/n junction of the diodes. The p^+ region was formed either by ion implantation or by diffusion; and optionally, additional lattice damage was created by silicon ion implantation. The experiments presented in this chapter clearly indicate that lattice defects have a detrimental effect on the efficiency of light emission from silicon light-emitting diodes (Si LEDs).

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Tu Hoang, et al., *The Effect of Dislocation Loops on the Light Emission of Silicon LEDs*, Proc. of ESSDERC 2005, pp. 359–362, Grenoble, September 2005.

Tu Hoang, et al., *The effect of Dislocation Loops on the Light Emission of Silicon LEDs*, IEEE Electron Device Letters, vol. 27, no. 2, pp. 105–107, February 2006.

Introduction

Ion implantation has been the dominant doping technique for silicon ICs since the late 70-s. Ion implantation proceeds through accelerated ions shot into a perfect silicon lattice, each implanted ion creating a cascade of damage displacing numerous silicon atoms [1] with crystal damages as a consequence. Recently, ion implantation has been proposed by Ng *et al.* [2] as a key technique to improve the light emission property of Si. In that paper Boron-ion implantation was used to fabricate light emitting diodes with a dislocation loop region close to the p/n junction. It was shown by Ng. that the internal quantum efficiency of such diodes can reach 10^{-3} at room temperature. The higher efficiency of light emission is attributed to the presence of dislocation loops near the p/n junction. It is argued that these loops spatially confine carriers through a modification of the band structure, thus reducing the probability that carriers recombine through a non-radiative process at point defects in silicon.

However, this explanation of the observed relatively strong light emission has led to debate in literature [3-10]. By texturing the silicon wafer surface with inverted pyramid structures in combination with minimizing parasitic recombination by using high purity float-zone silicon wafers, Trupke *et al.* [5] recently showed that high purity bulk crystalline silicon may have a much higher light emission efficiency (6.1 $\%$ external photoluminescence quantum efficiency at room temperature) than assumed thus far. Kittler *et al.* [6] claimed that the efficiency for light emission is largely governed by the Shockley-Read-Hall (SRH) lifetime τ_{SRH}, i.e., the quality of the Si material. In nearly *perfect* Si material the maximum quantum efficiency η is expected to reach about 30 $\%$! Stowe *et al.* [7] reported on experiments where boron or silicon was implanted to form defects in silicon. These experiments showed that light emission occurs in damaged silicon samples even when no p/n junction is present. Furthermore, Sobolev *et al.* [9] used Boron implantations to fabricate p/n junction on n-Cz-Si substrate and the highest electroluminescence efficiency in those experiments was obtained when there are no extended defects which means no observation of the effect of the spatial carrier confinement in their experiments.

In experiments from reference [4], the p/n junction was realized by diffusion in order to avoid introducing crystal damages, i.e., to yield high minority carrier recombination lifetimes in bulk silicon. Together with other techniques as in [5], the authors were able to reach $\sim$1 $\%$ external efficiency power conversion at room temperature. This led us to the idea of comparison of electroluminescence efficiency of Si LEDs fabricated with ion-implantation to that realized with dopant-diffusion. This will give more essential information about effects of dislocation loops on the light emission from silicon.

When dislocation loop engineering can really enhance the radiative recombi-

nation in Si LEDs, this would give potential for light-sources in silicon.

The experiments we carried out here can contribute in finding a suitable model, closer to reality, to explain what happens exactly inside the silicon light emitting diodes when the carriers are injected through these dislocation loop arrays.

4.1 Defects formation in Si-crystals by implantation

The implantation process used in Si-ICs consists of the acceleration of ions, targeting them at the silicon substrate thus implanting them into it. Each implanted ion itself follows a random trajectory with a range R, but the concentration of ions will peak at a projected depth R_{p} below the surface of the wafer. The spread of the ions depends on the traveling range; a deeper range allows for more random stopping events. This gives rise to a distribution of ions where most of the ions are within a standard deviation $\pm\triangle R_{\mathrm{p}}$ of the projected range R_{p}. The total number of ions implanted per cm^2 is defined as the dose and a convenient relationship between dose *Q*, peak concentration C_{p} and standard deviation $\pm\triangle R_{\mathrm{p}}$ can be derived by several models. The simplest model to calculate a 1D-distribution of implanted ions is the symmetric Gaussian implant model [11] as expressed in equation 4.1:

$$C(x) = C_{\mathrm{p}} \exp\left(-\frac{(x-R_{\mathrm{p}})^2}{2\triangle R_{\mathrm{p}}^2}\right) = \frac{Q}{2\pi\triangle R_{\mathrm{p}}} \exp\left(-\frac{(x-R_{\mathrm{p}})^2}{2\triangle R_{\mathrm{p}}^2}\right) \qquad [\mathrm{cm}^{-3}]. \tag{4.1}$$

Due to the effect of channeling, a tail of the implant profile can be formed much further than expected. Also lighter ions have the tendency to back scatter from silicon atoms and fill in the front side of the distribution. All these effects are included in the dual Pearson model [12], [13].

The equation (4.1) is also useful for calculating an effective thickness of a layer to be used as a mask to block the transmission of the implanted ions through it.

The scattering events can be divided into nuclear collisions and electronic stopping. Sharp nuclear collisions result in displacement of silicon atoms from the lattice sites. An atom or ion that does not reside at a lattice site, whether it is the displaced silicon atom or the implanted ion, is called *interstitial*. A silicon atom displaced from its own lattice site is called *self-interstitial*. The vacant lattice site is called *vacancy*. When an interstitial is injected into the lattice, considerable energy is released and the lattice becomes strained. The energy required to move the interstitial is low and the interstitials can easily migrate into energy sinks. Also impurity ions/atoms both in lattice and interstitial positions can act as a sink for lattice defects thus promoting the defect clustering processes. Interstitial

positions are matrix places between lattice sites [14]. However, when an amount of energy called the displacement energy, E_{d}, is put into the nuclear collision, a stable self-interstitial-vacancy pair is formed, the so-called Frenkel-pair. For silicon the displacement energy is approximately 15 eV. The implant energy E_{n} is often in the range of kilo-electronvolts (1–1000 keV). Therefore a large number of displacements will be introduced. A large amount of interstitials and vacancies are injected into the matrix. When interstitials or vacancies encounter each other they form clusters. Cluster formation reduces the amount of dangling bonds and is therefore energetically favored. So the resulting lattice defects are primarily small interstitial and vacancy clusters. The recombination of a vacancy and interstitial restores the lattice-order. If the dose is high enough the primary damage builds up until eventually an amorphous state is reached. The threshold for amorphous layer production is the total vacancy concentration above which the substrate is assumed to be amorphous. It is expressed as a percentage of the silicon atom concentration [1]: the silicon atom concentration is 5×10^{22} ions/cm^3, and this threshold is often taken to be within 10 $\%$ of the silicon lattice density.

The forming of an amorphous layer is almost exclusively dictated by the implant dose. However, the subsequent evolution of the amorphous layer depends upon the implanted atom/ion mass and implantation energy. As pointed out in [1], for heavy ions like arsenic, whose stopping may be dominated by nuclear collisions, the damage profile is relatively flat over the whole projected range up to R_{p}, i.e., from surface to projected range atoms have been displaced. Lighter ions like boron have an appreciable component of electronic stopping at higher energies. Electronic stopping does not result into displacement of atoms. Therefore, the damage accumulation is concentrated near R_p, i.e., atoms are only displaced near R_{p}. For lighter ions then, the amorphous region will form first at the peak of the damage density profile near R_{p} and expands on both sides of this depth as the implanted dose is increased.

During the ion implantation, various levels of damage can be introduced to the lattice. Due to the presence of large amounts of interstitials in this region, the lattice becomes stretched. Meanwhile, the Solid Phase Epitaxy (SPE) re-growth is not stretched. Therefore, high stress exists at the amorphous-crystalline interface. To relieve stress, interstitials just beyond the amorphous-crystalline interface form dislocation loops. The nucleation process of dominant defects depends on implantation parameters (dose and acceleration energy) and post-annealing conditions like temperature and time. A *classification scheme* consisting of five categories for the different forms of implant-related damages was pointed out by Jones *et al.* in [15]. Many different configurations of dominant defects were classified and visualized by different techniques as shown in [16], [17], [18] and [19]. From our experiment, we intend to introduce dislocation loops on category II (or End of Range) damage with two configurations: (perfect) prismatic dislocation loops

and faulted-Frank dislocation loops, those are shown in the following sections.

The category II damages cannot be avoided once an amorphous layer is formed evolving into extrinsic dislocation loops after epitaxial regrowth of the amorphous layer at 550 °C and additional higher temperature treatment. The region occupied by the amorphous layer is negatively strained after annealing whereas the category II regions are positively strained because of the extra concentration of interstitials in those regions. There is still a strain field at the dislocation loop regions although the energy reduction was associated with formation of a large interstitial cluster. Therefore, they can behave as gettering sites for impurities and implanted dopants.

The loop growth is governed by the bulk-diffusion mechanism. According to bulk diffusion mechanism, the radii of growing loops are proportional to the annealing time. This implies a uniformly increasing average loop radii. In addition, the loop growth rate increases with the increase of annealing temperature. At lower temperatures (700 °C, 800 °C) this growth appears to be much slower than that at high temperatures (900 °C, 1000 °C). In general, secondary defects become large enough during post implantation annealing at temperatures exceeding 700 °C in order to be observable via transmission electron microscopy (TEM). In the meantime of the growing dislocation-loop sizes with temperature, the total loop density is decreasing. For 700 °C and 800 °C annealing, the loops remain in the coarsening regime and the density of the interstitials bound by the loops is constant during the annealing process. For 900 °C annealing, the interstitial density decreases after 30 minutes and the loops change from the coarsening regime to the dissolution regime. After only 15 minutes of annealing at 1000 °C, the loop dissolution process starts and the interstitial density reaches a very small value ($< 3 \times 10^{12}/\text{cm}^2$) after 2 hours. For annealing times greater than 2 hours at 1000 °C, very few loops remain and they evolve into stacking faults [20–22].

4.2 Experimental

In order to analyze the influence of the dislocation loops on the luminescence from silicon, we fabricated p^+n diodes in Cz-grown 5–10 Ωcm n-type silicon wafers, with the p^+ located near the silicon surface (see Figure 4.1). The p^+ region was formed by either B^+ ion implantation (at various energies between 40–100 keV) or by solid-state diffusion from B-doped CVD oxide layers. The dislocation loop formation inside the B-implanted LEDs was controlled by varying the temperature of post-annealing between 850–1000 °C, for 20 minutes (in line with Ng *et al.* [2]). The diodes formed by B diffusion were optionally implanted with silicon (10^{15} Si^+ atoms/cm^2 at 200 keV and/or 450 keV) and subsequently annealed at 950 °C for 20 minutes after each implantation to form dislocation loops. Two implant energies of silicon were used to control the depth of the dis-

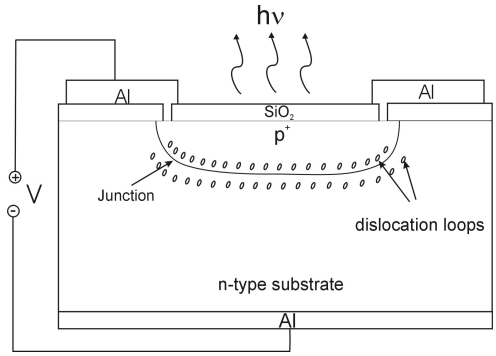

Figure 4.1: Solid schematic of structure of the fabricated LEDs.

location loops: either before the metallurgical junction, i.e., inside the p^+ region (using 200 keV) or beyond it, i.e., in the n region (with 450 keV). The conditions used, such as: implantation dose, acceleration voltage, annealing temperature and time, are suitable for forming process of the category II dislocation loops. The silicon implants were carried out on half of the wafer only: the 450 keV implant was carried out on the right half, whereas the 200 keV implant was carried out on the bottom half, as sketched in Figure 4.2. In this manner, the comparison between implanted and non-implanted diodes becomes more representative since all diodes are bound to exactly the same process conditions. After implanting and

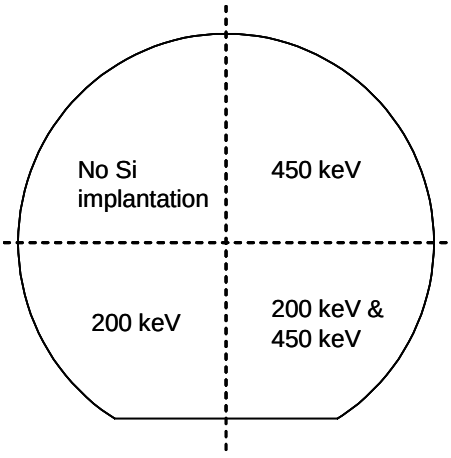

Figure 4.2: Silicon ion implantation experiments on a single wafer containing B-diffused silicon LEDs.

annealing, aluminum contact pads were formed at the back- and front-sides of the device. The wafers were then sintered at 400 °C for 5 minutes in wet N_2. In order to get comparable diodes, the sizes and structures of the fabricated LEDs were

taken identical. The p^+ sheet-resistance and junction depth were controlled to be in the same range by changing implantation energy and diffusion conditions. The sheet-resistance of the p^+ regions was measured by the *four-point* method, and the junction depth of the p^+/n junctions was checked by the *"ball-grooving"* technique. The obtained junction depth (X_j) and sheet resistance ρ_s of all LEDs are presented in table 4.1.

Nr.	p^+ formation	Si^+ implant (10^{15} cm^{-2})	Anneal	$X_j \pm 50$ (nm)	$\rho_s \pm 0.4$ ($\Omega/\square$)
1	diffusion	–	2 × 20' 950 °C	415	25.0
2	diffusion	200 keV	2 × 20' 950 °C	410	25.0
3	diffusion	450 keV	2 × 20' 950 °C	410	24.7
4	diffusion	200&450 keV	2 × 20' 950 °C	410	25.5
5	40 keV B^+	–	20' 850 °C	360	23.0
6	40 keV B^+	–	20' 900 °C	370	23.7
7	40 keV B^+	–	20' 950 °C	395	24.7
8	40 keV B^+	–	20' 1050 °C	420	25.2
9	100 keV B^+	–	20' 950 °C	650	28.2

Table 4.1: Overview of the silicon LED process variations and the measured data of the junction depth (X_j) and the sheet resistance (ρ_s) for these LEDs. Samples with p^+ region made by B-diffusion are annealed after each of the silicon implants.

These parameters of both implanted- and diffused-diodes have been used as one of the key-elements for getting the suitable experimental conditions to realize the comparable devices. The lateral extension of the p^+ region is typically 200 × 200 μm^2.

Electrical characteristics were measured using a Cascade probe station and an Agilent 4156C parameter analyzer. Emission spectra were obtained with a Spectro 320 scanning spectrometer and an InGaAs detector. An optical fiber (65 μm diameter) was mounted on a micromanipulator and positioned above the LED to guide the light from the LED to the spectrometer. This detector with sensitivity in the range of 850–1650 nm is very suitable for the emitted spectra centered around ∼1100 nm wavelength. The EL efficiency measurements were carried out at IHP/BTU Jointlab, Cottbus, Germany, with a cooled Ge detector.

The presence of extended defects was verified using HR-XRD and HRTEM measurements. The strain profile, created by the appearance of dislocation loops, in Si crystalline has been obtained by HR-XRD using the program X'Pert Epitaxy v.4.0 from Panalytical B.V. And the configurations of the introduced dislocation loops were observed by HRTEM images. More details about equipment and measurement procedures are explained in chapter 3.

4.3 Configurations and strain profile of defects

Configuration and presence of lattice defects created in both B-implanted and Si-implanted devices were investigated by cross-section TEM analysis. From all TEM images it is obviously seen that the dominant defects are dislocation loops. Actually, there is also the existence of other kinds of defects such as dislocations and point defects but very little compared to dislocation loops. The two configurations of the formed dislocation loops that can be seen in all TEM images are faulted Frank loops and prismatic loops.

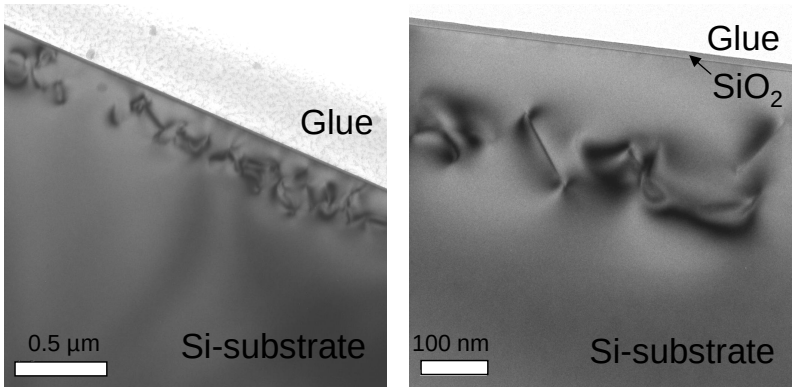

Figure 4.3: Two magnifications of cross-section HR-TEM of a B-implanted device with 40 keV implantation energy followed by annealing at 950 °C for 20 minutes in nitrogen.

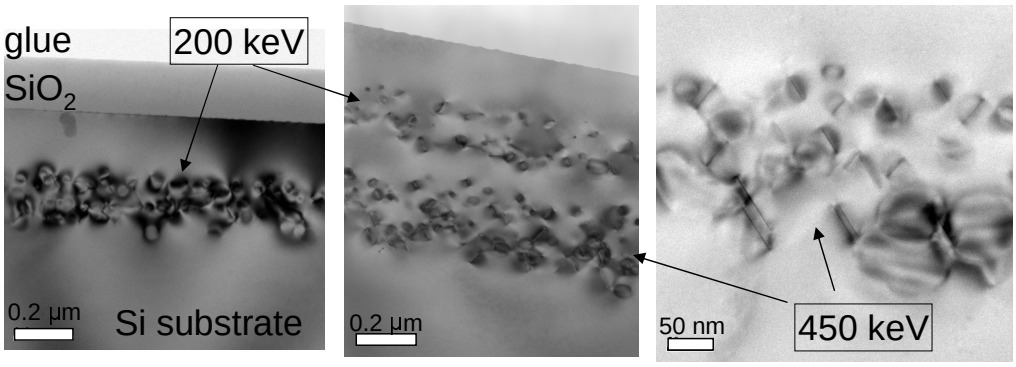

Figure 4.4: Cross-section HR-TEM of three Si-implanted devices: implantation energy at 200 keV (*left*); at 450 keV (*right*) and two implantation levels 200 keV + 450 keV (*middle*) with post-annealing at 950 °C for 20 minutes in nitrogen.

In the B-implanted devices, dislocation loops were created in the upper 300 nm of the sample as shown in Figure 4.3. The defects do not extend to the upper

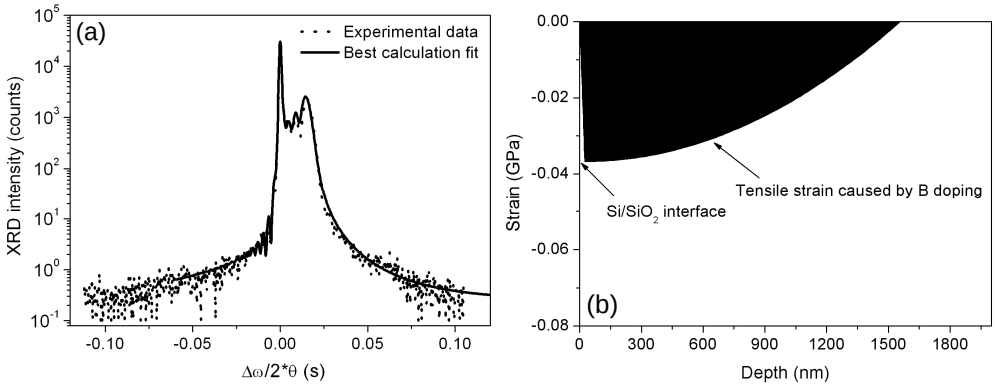

Figure 4.5: HXRD profile depends on scan-angle of B-diffusion specimen without implantation. In (a): the dot-line is the experimental HRXRD intensity as function of scanning angle; and the continuous-line is the best fit corresponding to the calculated data from simulation model of the XRD technology. In (b): Strain profile dependence from depth of sample obtained by simulation corresponding to the best-fit data; Only tensile strain introduced by boron dopant extending deeply into the silicon substrate.

Si/SiO_2 interface. Since boron implantation was used to fabricate p^+ regions and also to introduce dislocation loops, the p/n junction will locate deeper into the silicon substrate. Using the ball-grooving technique on the fabricated structure we see the p/n junction at 395 nm $\pm$ 50 nm depth from the Si/SiO_2 interface.

The dislocation loops were also observed on Si-implanted devices realized at different implantation energies as presented in Figure 4.4. The band of defects is present at a depth of 250–350 nm and of 450–670 nm below the Si/SiO_2 interface respectively for 200 keV and 450 keV Si-implanted sample. The dislocation-loop band formed by silicon implantation expands into a larger range and has a higher density with respect to that in the boron implantation samples because of heavier implanted-ions and higher implantation energy. However, the diameter of dislocation loops in both Si and B-implanted samples are similar and in the range of $\sim$100 nm, since they were formed in the same post-annealing conditions. These profiles of dislocation loops can also be seen in TEM image of devices with two implantation energy levels as shown in the middle of Figure 4.4.

The junction depth on the Si-implanted devices have also been determined by using the ball-grooving technique. At a depth of $\sim$410 nm, the p/n junction is located between the two dislocation-loop arrays formed by 200 keV and 450 keV implantation.

High resolution X-Ray diffraction technology was used in order to quantitatively extract the strain-field profiles introduced by the existence of dislocation loops in crystalline silicon. The measurement results obtained from the non-implanted and from the 200 keV Si-implantation sample are shown in Figure 4.5

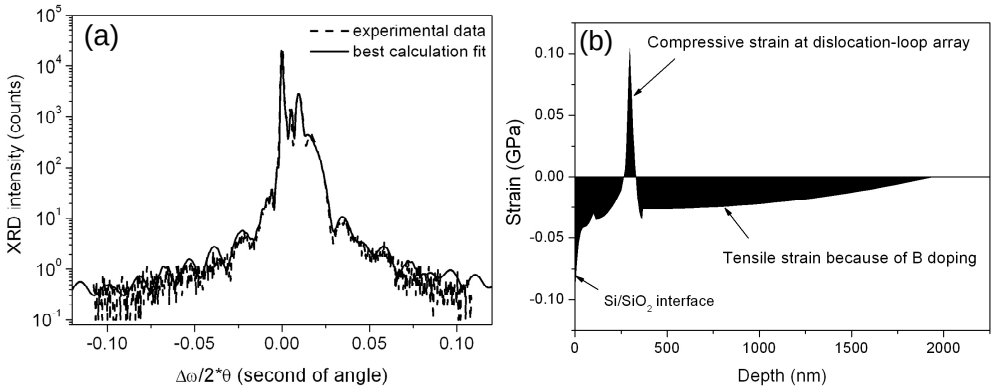

Figure 4.6: (a): HXRD profile depends on scan-angle from B-diffusion specimen with Si-implantation at 200 keV. (b): Strain profile dependence from depth of sample obtained by simulation corresponding to the best-fit data; A compressive strain peak of ∼0.1 GPa (da/a = 800 ppm) is created by presence of dislocation loops at 250–320 nm depth from Si/SiO_2 interface.

and Figure 4.6, respectively. In both Figures the dotted line is the experimental XRD intensity in counts as a function of scanning angle ($\Delta\omega/2\theta$) in seconds, and the continuous line is the best fit corresponding to the calculated data from the simulation model of the XRD technology. According to these calculated data a simulation was carried out to extract the strain profile around dislocation-loop arrays. The absolute magnitude of this strain was calculated by using *Hooke's* law:

$$\sigma = Y_{\mathrm{Si}} \cdot \frac{\mathrm{da}}{\mathrm{a_{Si}}} \tag{4.2}$$

where Y_{Si} is Young's modulus of crystal silicon at 300 K, 113 GPa, $\mathrm{da/a_{Si}}$ is the relative strain of silicon, and $\mathrm{a_{Si}}$ is the lattice unit of silicon, 5.43 Å.

A tensile strain, as a result of boron doping, is extending from the Si/SiO_2 interface to deeply into the silicon substrate and is observed on both samples. A compressive strain peak of ∼0.1 GPa (corresponding to da/a = 800 ppm and in the same magnitude level as presented in [24]) created by the presence of dislocation loops at 250–320 nm depth from Si/SiO_2 interface is only observed in the Si-implanted sample as shown in Figure 4.6b. The position of this strain peak is in agreement with the position of the dislocation loop array on the HRTEM micrographs of that sample.

4.4 Electrical Characteristics

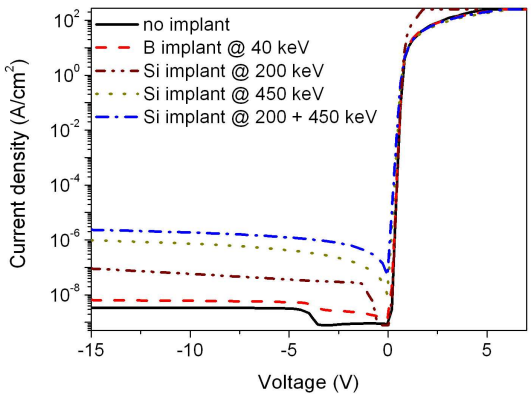

Figure 4.7: J-V characteristics of five LEDs: B-diffused without implant; B-implanted at 40 keV; B-diffused with Si implant at different energy 200 keV, 450 keV, 200 + 450 keV. All LEDs were annealed in nitrogen at temperature of 950 °C for 20 minutes.

Current density-voltage *(J-V)* characteristics were measured at room temperature between the back and front contacts to verify a normal diode operation and to investigate the level of generation-recombination currents. All devices show a low leakage current, as illustrated in Figure 4.7 for five diodes with the same size but different defect densities. This is contrary to the result described in reference [2]. At a reverse-bias of 15 V, the highest leakage-current density of 2.5 μA/cm^2 was seen in the doubly implanted diode. Under forward bias, for every decade change of current, the voltage changes vary in the range of 64 mV to 72 mV, and the dominant contribution to the total current is the diffusion current component. It means that all diodes show a good ideality and recombination process takes place outside the space charge region throughout the low injection regime.

4.5 Light Emission Properties

The electroluminescence measurement of the devices was carried out at room temperature. Electroluminescence was observed under forward bias at a constant current of 100 mA (current density of 250 A/cm^2). Light comes out not only straight above the diode itself, but also (with weaker intensity) from the sides, as shown by the photograph in Figure 4.8, and also reported in [2].

The LED efficiencies were estimated from the EL band-to-band transition peaks. The spectra were normalized using the spectral response of the system on a calibrated light source. The normalized spectra were then integrated and

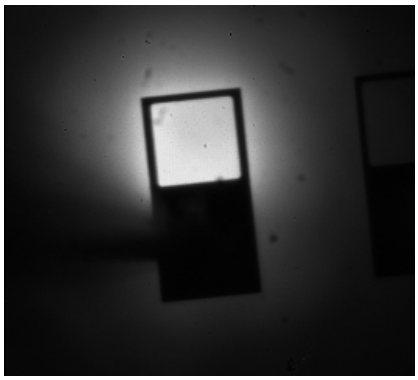

Figure 4.8: Photograph of a silicon LED device under a forward bias current of 50 mA, taken with an InGaAs (infrared) camera. The inside square is the diode area; the rectangular black feature around it is the aluminum interconnect and bond pad.

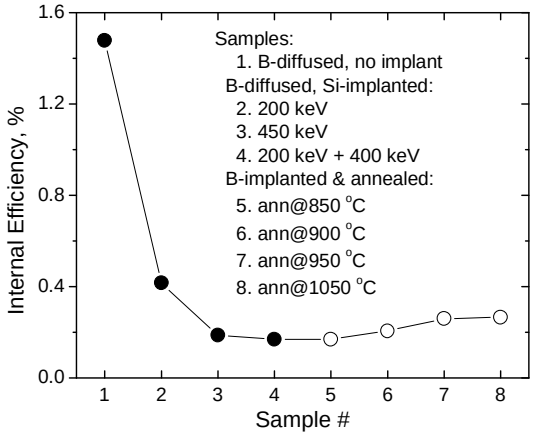

Figure 4.9: Comparison internal efficiency of all diodes.

after which the values were converted into photon flow at the energy of the related peak maxima and divided by the acting value of electron flow to obtain the external quantum efficiency. A correction factor of 73 between internal and external quantum efficiency was calculated with the assumption of a Lambertian cosine distribution of emission from the diode surface and an ignorable contribution from the reflection of the wafer-backside [6] [25]. The experimental error of these absolute measurements was estimated to be about 30 $\%$ and was mainly due to inaccuracy in adjustment of samples, mirrors, and calibration sources. The estimated internal efficiency of all diodes are compared and shown in Figure 4.9. A maximal internal efficiency of 1.5 $\%$ was demonstrated by the B-diffused (without implantation) diode. The diode with double Si-ion implantation of (at 200 KeV and 450 keV) shows the lowest efficiency. The efficiency of B-implanted samples

was significantly below the value for the diffused LED and those improved with the increase of annealing temperature.

All electroluminescence spectra of the manufactured LEDs show the same emission peak at a wavelength of around 1150 nm, associated with phonon-assisted radiative band-to-band recombination.

4.5.1 B-implanted LEDs

The evolution of the dislocation loops depends on the annealing conditions after implantation as pointed out in the first section. In Figure 4.10 the emission spectra of B-implanted LEDs annealed for 20 minutes at four temperatures are displayed. The highest light emission intensity is found in the device annealed at 1050 °C, consistent with the reported trend in [9]. Identically processed devices showed a 4.3 % variation of the electroluminescence.

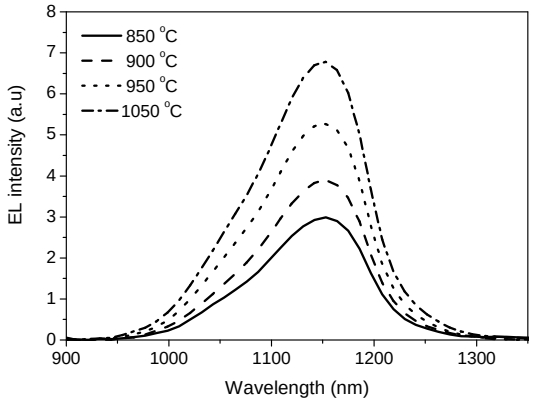

Figure 4.10: Emission spectra of B-implanted LEDs under 100 mA bias current as a function of wavelength, annealed at various temperatures.

Figure 4.11 also shows a clear difference between light emission from shallow and deep junctions. The light intensity increases with a deeper boron implant. A higher energy implant leads to a deeper junction, and therefore minority carrier injection takes place deeper into the bulk. As a result, non-radiative interface recombination is more significant in the shallow junction LED than in the one with the deeper junction. Moreover, the recombination rate at the p^+ contact also plays an important role in these devices (see chapter 2). Since in the shallower junction the dislocation-loops are closer to the junction, they attract more recombination at the p^+ contact and thus a lower injection level in the bulk. These two reasons explained for the observation shown in Figure 4.11 and were supported by previous reports [5].

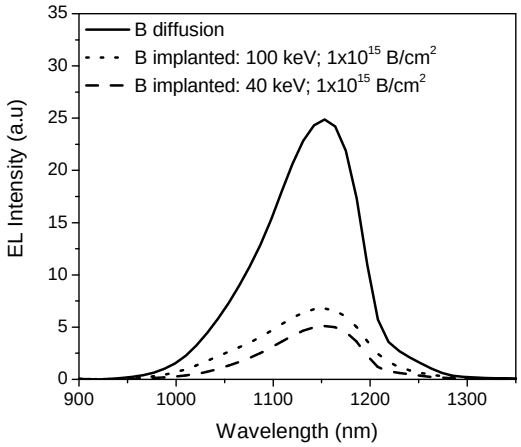

Figure 4.11: A silicon LED formed by diffusion exhibits stronger light emission than an ion-implanted LED. A lower implant energy leads also to lower light emission.

A direct comparison of LEDs with the same physical properties but prepared to use boron diffusion rather than implantation, shows a surprising phenomenon. The spectra obtained from these compared LEDs are shown in Figure 4.11. Whereas the light emission spectra from these two types of diodes show the same form, indicating the same root for the photon emission mechanism, the intensity of electroluminescence is higher for the diffused diodes than for the implanted ones! This strongly indicates that the defects created in the silicon (by the boron implant) influence the light emission in the diode; they reduce rather than enhance it.

In earlier work [2], it was assumed that the light emission in silicon is enhanced by the presence of dislocation loops, through the formation of a strain field. From the experimental results presented above, however, it seems that the introduction of dislocation loops suppresses the radiative recombination! For an independent confirmation of this remarkable result we set up a second experiment, which will be presented in the next section.

4.5.2 B-diffusion LEDs with and without Si implantation

The same LEDs formed by boron diffusion, i.e., diodes with negligible crystal damage, were exposed to silicon implantations and subsequently annealed (before metalization). An appropriate choice of annealing temperature and time (950 °C and 20 minutes) results into the formation of extended defects close to the diode junction. Cross-section TEM micrographs confirmed the presence of the dislocation loops at the appropriate depth, as indicated in section 4.3. The dislocation loop density was estimated to be 5×10^{11} cm^{-2} in the silicon-implanted samples,

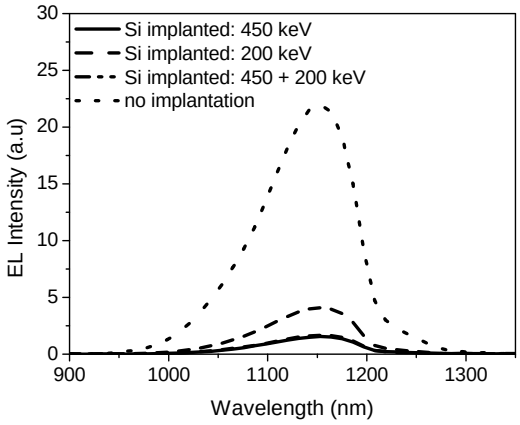

Figure 4.12: Comparison of the electroluminescence of B-diffused silicon diodes without, and with silicon ion implantation to form lattice defects. The device with the least lattice damage emits most light.

which is more than three orders of magnitude higher than the density observed in diffused junctions [26]. It means that the effect of crystal defects introduced on the diffused LEDs by diffusion process consequently is three orders smaller than that on the implanted LEDs. In experiments from Green *et al.* [4], dopant-diffusion technology is used and is one of the important elements for getting improvement of electroluminescence from silicon diodes.

This experimental approach leads to very similar silicon-based LEDs with and without silicon lattice damage. The spectra obtained from these diodes confirm our earlier findings, see Figure 4.12. Diodes that received no implant exhibit the highest electroluminescence; implantation forming defects above the junction has a detrimental effect to the luminescence, but the deeper defect implantation (450 keV) is clearly the most detrimental to the light emission. These experiments provide support for the earlier suggestion by Sobolev *et al.* [9] that gettering of recombination centers might play a role in the improvement found by Ng *et al.* [2], and the recent findings of Trupke *et al.* [5] that clean, monocrystalline silicon may be a much more efficient light source than generally assumed. With our experimental method, we were not able to separate the effects of different defects (point defects, dislocations, stacking faults...) to the emission efficiency, and one type of defect may counteract the contribution of another. However, since the mechanisms for the evolution process of dislocation loops as pointed out before in the first section and the fact of the obtained data, the dominating defects, present close to the p/n junction in the fabricated LEDs, are dislocation loops! Therefore, on high quality monocrystalline silicon material, where the cleaning-function of the gettering processes is less important, dislocation loops mainly affect the radiative

recombination rate due to a lower injection level caused by the additional SRH recombination at the defects.

The appearance of strain fields in crystalline silicon at the dislocation loop region helps to create an energy sink that acts as gettering centers for impurities and implanted dopants, and the carrier confinement function of that strain field has not been observed in these experiments. Furthermore, the presence of dislocation loops close to p/n junction of LEDs creates extra non-radiative recombination centers at a deep state [27] which considerably decreases the light emission efficiency.

4.5.3 Temperature Effects

The temperature dependence of the light emission spectra was investigated by measurements at various chuck temperatures in the range of 253–473 K. Three diodes were characterized: one boron-implanted and the other two boron-diffused diodes with and without silicon implantation. A monotonous increase of the integrated electroluminescence with temperature, shown in Figure 4.13, is found in all diodes with and without dislocation loops.

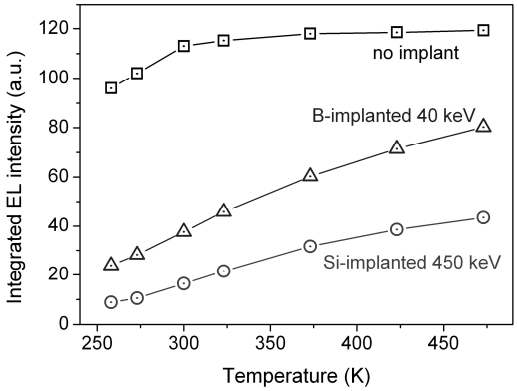

Figure 4.13: Integrated EL intensity as function of chuck temperature in range 253–473 K: B-diffused diode (square symbol); B-implanted LED at 40 keV (triangle symbol) and B-diffused LED with Si implant at 450 keV (circle symbol).

The temperature dependence of emission from silicon LEDs received much attention regarding the essential physics behind it. However, conflicting observations were presented in literature. In particular at the temperature range above 200 K contradicting results were reported. In [6] and [31] an increasing EL was observed with increasing temperature; in [2] the EL was rather independent of temperature in that range; and in [4] an opposite behavior, i.e., decreasing EL with increasing temperature, was observed.

With the model proposed in [6], the SRH statistics for shallow-trap levels were used and the increase of SRH lifetime with temperature was obtained. When the excess carrier concentration $\Delta n < 10^{17}/cm^3$, the SRH-lifetime increase could overcompensate the decrease of the radiative recombination coefficient. Thus, the SRH-lifetime increases when temperature increases corresponding to an increase of the light emission efficiency η(T). However, since in our experiments the luminescence was observed at high injection levels (i.e., at higher excess carrier concentration), this model may not be applicable.

In [31] the authors reported another model based on the fact that when a p/n junction was present in a silicon substrate, there are two different radiative recombination processes occurring competitively: the transverse optical (TO) phonon-assisted free exciton recombination at band-edge of silicon, and the TO phonon-assisted of excitons bound to traps. Redistribution between these two processes when raising the temperature led to the anomalous temperature behavior of the light emission from silicon light emitting diodes. This model showed a very good fit with their experimental results. But, from our observations (and also from [3, 5, 6]), the radiative band-to-band recombination process occurs mostly deeply in the silicon substrate, far from the p/n junction (i.e., far from the created defects). Thus this model is probably also not suitable to explain the temperature behavior in our experiments. We should, however, keep in mind that an increasing recombination rate at the p/n junction will influence the injection level in the bulk when operating at constant current.

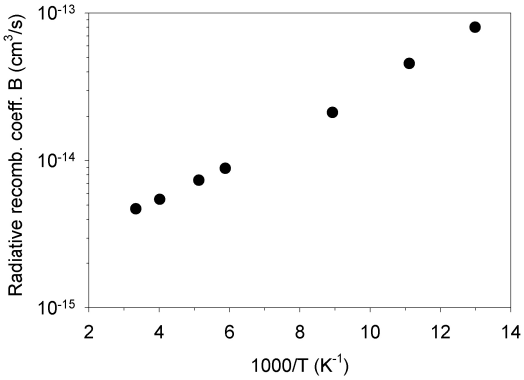

Figure 4.14: The band-to-band radiative recombination coefficient B versus 1000/T, data extracted from [29].

We have to realize that the band-to-band radiative recombination rate coefficient B depends not only on temperature but also on the injection level [25, 26, 29]. At different temperatures, the decrease of B when increasing the injection level occurs with different temperature dependent rates [32]. The B-values at low

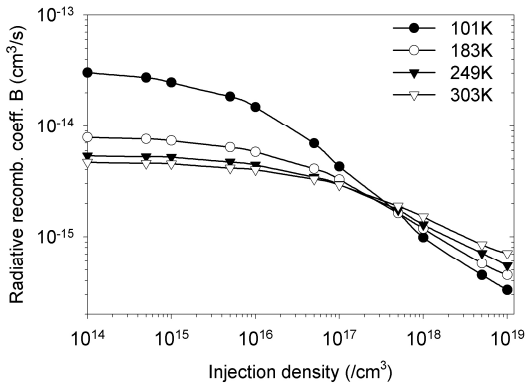

Figure 4.15: Decease of band-to-band radiative recombination coefficient B with injection density at different temperatures, data extracted from [29] and [32].

injection level were taken from [29] and combined with the results from [32], see Figure 4.14. When we combine the data from [29] and [32] we can calculate the decrease of B with injection density at different temperatures as shown in Figure 4.15. We can clearly see that when the injection density is below $\sim 2 \times 10^{17}$ /cm^3, B decreases with increasing temperature and vice versa above $\sim 2 \times 10^{17}$ /cm^3. This explains the contradicting experimental temperature observations as mentioned above and the positive temperature behavior which we observed.

We should further keep in mind, as mentioned in chapter 2, that at this high injection level, the carrier lifetime is controlled by the Auger recombination process and that the Auger recombination rate coefficient increases with increasing temperature [33]. Due to this the injection level will increase for increasing temperature at constant injection current. These two phenomena fully clarify the EL temperature dependence of our fabricated LEDs.

Spectra of one of three diodes, the boron-diffused diode with silicon implant at 450 keV, at different temperatures are given in Figure 4.16. That Figure also clearly shows the trend that the emission peak of all diodes shifts to larger wavelengths, qualitatively consistent with the band gap decrease as a function of temperature [34]. That change in band-gap energy of semiconductors can be expressed by the equation [27]:

$$E_g = E_0 - \frac{\alpha \cdot T^2}{T + \beta} \tag{4.3}$$

where E_0 is band-gap energy at 0 K; α and β are fitting parameters, for silicon they are 4.73 $\times$ 10^{-4} (eV/K) and 636 K respectively.

When the temperature increases up to 423 K an indent around the intensity peak of spectra was observed as in Figure 4.16. This can be explained by the

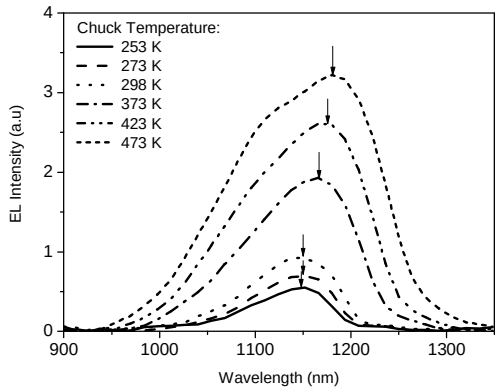

Figure 4.16: EL spectra of B-diffused LED with Si implant at 450 keV as function of chuck temperature in range 253-473 K.

change of the absorption coefficient of silicon at high temperatures and might be a result of competition at high temperatures between the two competing processes of photon emission and photon absorption.

Conclusion

Silicon light emitting diodes were reported to exhibit high quantum efficiency when the crystal defects are created near the p/n junction. However, with our two experimental approaches we show that silicon lattice damage has a detrimental effect to the emission of light in forward-biased silicon $p^{+}n$ diodes. This was observed in a wide experimentation range with varying dislocation loop densities, dislocation loop depth, and annealing temperature. This new finding contributes to a revision of the current understanding of light emission from defect-engineered silicon LEDs. In these experiments a presence of local carrier confinement close to dislocation loop regions due to the created strain field was not observed.

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Chapter 5

Band-edge and D-line emission from bulk Si LEDs

Abstract

The work carried out in chapter 4 is extended by the cooperation with a research group named IHP/BTU JointLab in Cottbus, Germany. The results obtained from the JointLab on our realized bulk Si-LEDs show that the light emission from silicon can be tailored to a longer wavelength at the telecommunications level by the formed dislocation loops. The main results were presented in the IEEE Transaction on Electron Devices. In this chapter we reprint this publication.

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Influence of Dislocation Loops on the Near-Infrared Light Emission From Silicon Diodes

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***Abstract*—The infrared light emission of forward-biased silicon diodes is studied. Through ion implantation and anneal, dislocation loops were created near the diode junction. These loops suppress the light emission at the band-to-band peak around 1.1 μm. The so-called D1 line at 1.5 μm is strongly enhanced by these dislocation loops. We report a full study of photoluminescence and electroluminescence of these diodes. The results lead to new insights for the manufacturing approach of practical infrared light sources in integrated circuits.**

***Index Terms*—Dislocation loops, integrated optics, integrated optoelectronics, light-emitting diodes (LEDs), light sources, luminescent devices, optoelectronic devices, semiconductor device fabrication, semiconductor devices, silicon.**

I. Introduction

INTEGRATED electronics and integrated optics are enabling technologies for the digital age. A breakthrough is expected when electronics and optics can be fully integrated onto a single chip [1]. Currently, light can be transported, split, switched, and detected using integrated components in a microchip. However, a light source that meets all the requirements for full monolithic integration is still being searched. The quest is for an efficient light source operating at (and above) room temperature and preferably emitting in a narrow wavelength range. Red or near-infrared light would be very suitable for communication purposes. The light emitter should be laterally confined and preferably switchable at gigahertz frequencies.

Light-emitting diodes (LEDs) and laser diodes based on III-V semiconductors show excellent technical qualities, but integration of these into a silicon chip has proved far from straightforward. The use of a silicon diode as LED is complicated by the indirect bandgap. This leads to a long lifetime for radiative recombination and, hence, severe competition from nonradiative recombination processes. Until only a few years ago, the quantum efficiency of a standard silicon diode was assumed limited to 10^{-6}. However, it was recently shown that forward-biased silicon diodes can reach an external quantum efficiency close to 1%, combining standard silicon technology with established techniques from the LED and solar cell industries [2]. The key in reaching high internal quantum efficiency is in the mastering of the competing nonradiative recombination processes: Schockley-Read-Hall (SRH), Auger, and surface recombination [3]. A theoretical maximum efficiency around 20% has recently been predicted for silicon LEDs by several groups [4], [5]. Modern IC technology offers a complete toolkit to make such diodes, and one can further benefit from the high purity of present-day silicon wafers. Silicon also can be prepared to emit at somewhat longer wavelengths, as illustrated in Fig. 1 (after [6]); the D1 peak around 1.5 μm is particularly fascinating for the purpose of optical communication.

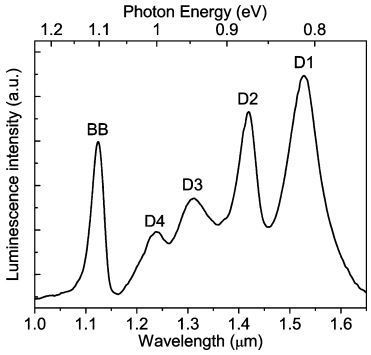

Fig. 1. Typical luminescence spectrum of dislocated Si measured at 80 K. The dislocation-related peaks D1–D4, as well as the BB peak, are indicated in the figure.

In various papers, a relation is reported between the quantum efficiency of such silicon LEDs and the presence of dislocation loops [6]–[10]. Dislocation loops can be conveniently formed using ion implantation and subsequent anneal. Therefore, a dislocation-loop-engineered silicon LED emerges as a potential light source for the further integration of electronics and optics. However, the contradicting reports in literature concerning the theoretical explanation of the dislocation loop's role,

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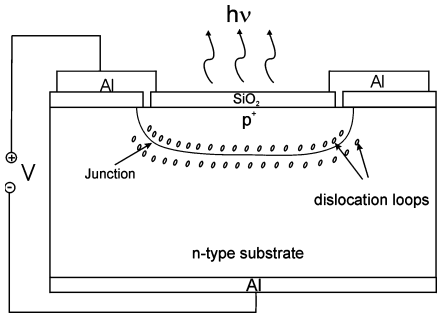

Fig. 2. Cross section of a LED with two dislocation loop arrays formed above and below the p^+/n junction.

as well as contrasting experimental reports, call for further experimentation.

In this paper, we investigated silicon LEDs with deep p^+–n junctions and created dislocation loops around the junction using ion implantation and anneal. In a recent paper [9], we presented evidence that dislocation loops are detrimental to band-to-band (BB) electroluminescence (EL). This paper brings a full account of photoluminescence (PL) and EL in the full wavelength region of interest (1–1.6 μm), which are extended to cryogenic temperatures. Also, further physical analysis using transmission electron microscope (TEM) and high-resolution X-ray diffraction spectroscopy (HRXRD) is presented. A complete and consistent physical picture emerges on the interaction between the dislocation loops and the light emission of silicon LEDs.

II. Experimental Details

A. Device Fabrication

We fabricated p^+n diodes in Cz-grown 5–10-$\Omega \cdot$ cm n-type silicon wafers (see Fig. 2). The p^+ region was formed by either 40-keV B^+ ion implantation or by solid-state diffusion from B-doped CVD oxide layers. The B diffusion took place at 950 °C for 10 min in nitrogen plus 20 min in oxygen. Under this condition, the p^+ sheet resistance and junction depth were in the same range as the B-implanted regions (around 25 Ω/square and 400 nm, respectively). The sheet resistance of the p^+ regions was measured with a four-point probe, and the junction depth of the p^+/n junctions was checked with the ball-grooving and staining technique. The dislocation loop formation inside the B-implanted LED was steered by varying the anneal temperature between 850 °C and 1050 °C, for a fixed time of 20 min.

The diodes formed by B diffusion were optionally implanted with 10^{15} Si^+ atoms/cm^2 and subsequently annealed at 950 °C for 20 min in nitrogen ambient to form dislocation loops. Two implant energies of silicon were used to control the position of the dislocation loops: either above the metallurgical junction, i.e., inside the p^+ region (using 200 keV) or beneath it, i.e., in the n region (with 450 keV). A single B-diffused wafer received all Si implant varieties, by implanting only part of the wafer.

TABLE I
Overview of the Silicon LED Process Variations. Samples 1–4 Are Annealed After Each of the Silicon Implants

Nr.	p^+ formation	Si^+ implant (10^{15} cm^{-2})	Anneal
1	diffusion	–	2 × 20' 950 °C
2	diffusion	200 keV	2 × 20' 950 °C
3	diffusion	450 keV	2 × 20' 950 °C
4	diffusion	200&450 keV	2 × 20' 950 °C
5	40 keV B^+	–	20' 850 °C
6	40 keV B^+	–	20' 900 °C
7	40 keV B^+	–	20' 950 °C
8	40 keV B^+	–	20' 1050 °C

Possible wafer-to-wafer variations (e.g., low-level contamination or thermal budget differences) are thus avoided. (Transient-enhanced boron diffusion caused by the silicon implants [11], [12] will result in slightly different p^+ profiles for each of the diodes. We found no evidence that this affects our results.) Under the given implantation dose, acceleration voltage, and annealing temperature and time, category-II dislocation loops form [13], [14] in two configurations: prismatic dislocation loops and faulted Frank dislocation loops.

Subsequent to the implantation and the final 950 °C anneal, aluminum was deposited at the front- and backside of the devices, and the front metal patterned. The wafers were then sintered at 400 °C for 5 min in wet N_2 ambient. The lateral dimensions of the p^+ region (approximately 200 × 200 μm^2) and the test structure geometry of the fabricated LEDs were similar for all those four regions as well as for the case of B-implanted samples. Larger areas were used for the PL measurements.

The details of sample fabrication are summarized in Table I. Variations were made in the formation of the p^+ region, the (optional) lattice-damaging silicon implant, and the thermal anneal. These experiments are intended to verify earlier experimental observations and to improve insight into the mechanisms behind these observations.

B. Measurement Setup

Electrical characteristics were measured using a Cascade probe station and an Agilent 4156C parameter analyzer. The EL was measured under current pulses (1–100 mA) with a frequency of ∼30 Hz. The PL from these samples was excited by an Ar-ion laser emitting at 514 nm with an excitation power of 100 mW and a laser-spot diameter of 100 μm. The excitation beam was chopped at ∼30-Hz frequency. For detection of EL and PL signals, the luminescence was analyzed with a monochromator and a liquid-nitrogen-cooled Ge detector system. A standard lock-in technique was applied to process the luminescence signals.

The LED efficiencies were estimated from the EL BB transition peaks. The spectra were normalized using the spectral response of the system on a calibrated light source. The normalized peaks were then integrated over wavelength. The obtained values were converted to photon flow values at the energy of related peak maxima and divided on the acting value of electron flow to obtain external quantum efficiency. The value for the internal efficiency was estimated by taking into consideration geometrical and reflectivity factors.

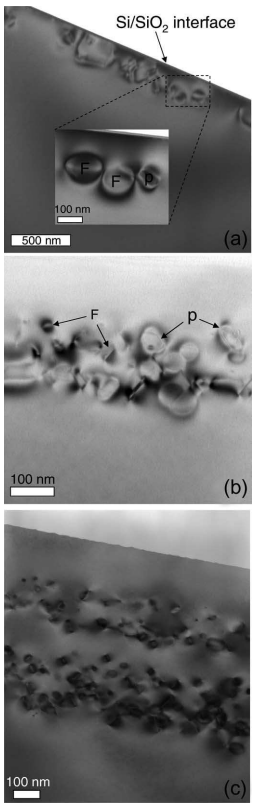

Fig. 3. HRTEM images of dislocation loops on the samples: (a) B-implanted at 40 keV; (b) Si-implanted at 200 keV; and (c) Si-implanted at 200 keV + 450 keV. The prismatic dislocation loops are indicated by the letter p, and the faulted Frank dislocation loops are indicated by the letter F.

III. Results and Discussion

A. Physical Analysis of the Dislocations

TEM images show that the dominant visible defects in the implanted samples are dislocation loops. In B-implanted samples, the dislocation loops were formed inside a 300-nm region from the sample surface, as shown in Fig. 3(a). In these samples, the implantation creates both the p^+ impurity profile and the lattice damage leading to dislocation loops. Since the dislocation loops form around the peak of the implantation profile (projected range) and always lie before the metallurgical junction, the p/n junction was located beneath the dislocation loops in the silicon substrate for B-implanted samples.

Dislocation loops were observed also in Si-implanted samples, as presented in Fig. 3(b) and (c). Bands of defects are present at depths of 250–350 and 450–670 nm below the Si/SiO_2 interface corresponding to 200- and 450-keV Si implantation, respectively. The density of dislocations is higher than in the B-implanted samples. The diameter of dislocation loops in both Si- and B-implanted samples was in the same $\sim$100-nm range. From the TEM images, it was obtained that the formed defects are mainly prismatic dislocation loops and faulted Frank dislocation loops (indicated in Fig. 3 by the letter p and F, respectively).

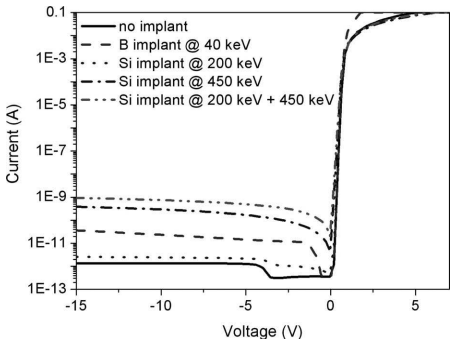

Fig. 4. I–V characteristics of five LEDs: B-diffused without implant; B-implanted at 40 keV; B-diffused with Si implanted at energies of 200, 450, and 200 + 450 keV. All these LEDs were annealed in nitrogen at 950 °C for 20 min.

By using HRXRD, the crystallographic features of the 200-keV Si-implanted sample were further investigated. As expected, the high boron doping results in tensile strain [15], extending almost 2 μm into the substrate. A compressive strain peak of 0.1 GPa $(da/a = 800$ ppm$)$, which is created by the presence of dislocation loops, is shown at 250–320-nm depth from Si/SiO_2 interface. The TEM and HRXRD results thus confirm that the silicon implantation and subsequent anneal caused dislocation loops in the desired regions.

B. Electrical Properties of the Diodes

Current–voltage $(I$–$V)$ characteristics were measured at room temperature between the back and front contacts to verify normal diode operation and to investigate the level of generation-recombination currents. The reverse leakage current of the B-diffused diode is very low. This indicates a low contamination level in our devices [16]. All B-implanted diodes also show low leakage currents. In the Si-implanted diodes, the leakage current was larger and increased with dislocation loop density, as shown in Fig. 4. However, the highest reverse-current density at -15 V of a double Si-implanted diode is still at the acceptable level of 2.5 $\mu A/cm^2$. Under forward bias, the diodes have a swing of 64–72 mV. This good ideality indicates that the recombination process predominantly takes place outside the space charge region throughout the low injection regime.

C. Diode Luminescence at Room Temperature

Infrared light emission is observed in all samples, both under forward biasing (EL) and when excited with an Ar laser (PL). Typical PL and EL spectra are shown in Fig. 5 (taken at cryogenic temperatures in this case). In most cases, the BB

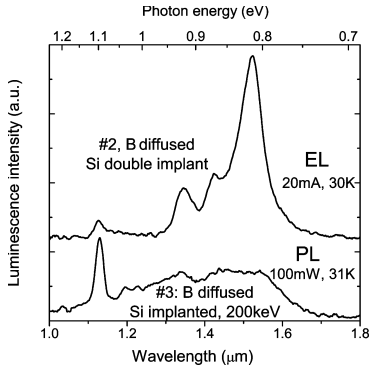

Fig. 5. Typical PL and EL spectra of samples, manufactured with boron diffusion and silicon implantation. The BB and D2–D4 peaks are observed in the spectra. At this low temperature, the D-band EL is dominant, because phonons are required for BB recombination.

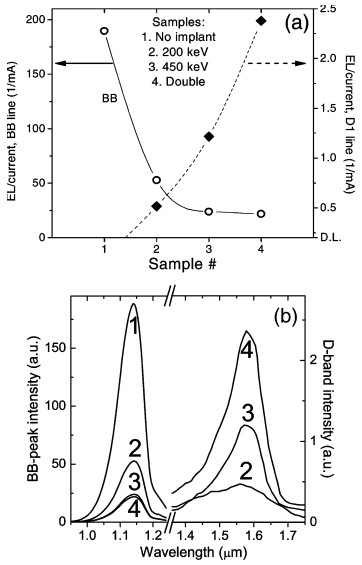

Fig. 6. Results of EL measurements on diodes made with B diffusion, optionally implanted with silicon. (a) The peak intensity of the BB and D1 lines for each of the samples. (b) EL peaks at these wavelengths. Measurements were performed at 300 K, and the diode forward bias was 20 mA.

recombination peak around 1150 nm and the D1 peak around 1500 nm are observed both in the PL and the EL spectra. With our measurements, we have confirmed that the intensity of both emission peaks depends strongly on the presence of silicon lattice damage, presumably the presence of dislocation loops. However, the trend is opposite: More lattice damage leads to an increase in D1 luminescence and a decrease in BB luminescence. This is quantified in Fig. 6. Concerning the BB peak, this result contradicts the assumption by Ng *et al.* [7] that dislocation loops are responsible for enhanced 1.1-μm light

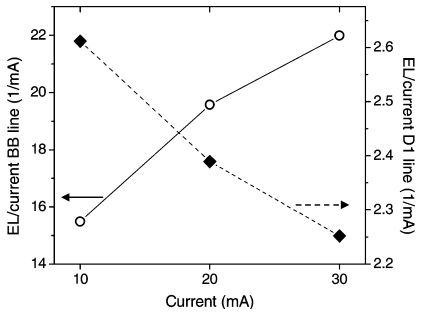

Fig. 7. Dependence of current-normalized EL intensities on the forward current. The data were obtained from a B-diffused double Si-implanted sample (sample 4 in Table I) at 300 K.

emission. This comes on top of earlier arguments [4], [17] that the carrier confinement mechanism proposed in those papers is not likely. Kveder also reported a decrease in BB luminescence in the presence of a high density of dislocation loops [8].

PL measurements confirm a strong BB signal on the B-diffused sample without silicon implantation. The signal from this sample was about 30 times stronger than that from the sample implanted with 200-keV Si^+ ions. In other silicon-implanted samples, at 300 K, the PL signal was below the detection limit.

Although our HRXRD measurements revealed the presence of a high strain field caused by the dislocation loops, no effect of the strain was detected on the BB luminescence peak position and/or shape. This result suggests that most of the BB luminescence originates far away from the loops. Therefore, BB radiative recombination mainly occurs in the defect-free regions of the wafer, as was suggested in [10].

All silicon-implanted samples exhibit D1 luminescence, as well as the B-implanted diode with lowest anneal temperature of 850 °C. Early studies of the lines D1–D4 indicated that the dislocation loops are responsible for the emission [18]. Indeed, we find an increase of D1 emission with increasing lattice damage (caused by silicon implants). Still, by using the implantation-damage approach, the D1 EL remains weak under all conditions. Plastic deformation of silicon, causing much higher dislocation loop densities, in combination with gettering and hydrogen passivation, led to external efficiencies of 0.1%–0.2% [8]—but plastic deformation is difficult to embed into microelectronic fabrication. Efficiency improvement for D1 emission could be feasible by using multiple implantation energies and special implantation geometries.

In Fig. 7, the ELs at the D1 and BB peak are shown in the forward-biased current range from 10 to 30 mA (at much higher injection than reported in [19]). The EL is normalized to current. Superlinear behavior is seen for the BB line, whereas the D1 line has a slight sublinear intensity increase with current. The BB efficiency thus improves at higher injection, whereas the D1 line is attenuating. The observed behavior of BB radiation is consistent with efficiency calculations as a function of the carrier injection level. The BB EL efficiency is expected to decrease at even higher injection levels (when the

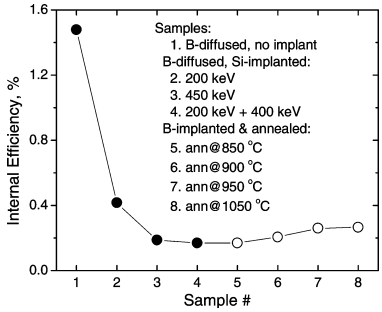

Fig. 8. Internal efficiency of various diodes, estimated from the external intensity of the BB peak at 300 K. Sample numbers are explained in the figure. Results from B-diffused samples are shown with closed circles, and B-implanted samples are shown with open circles.

carrier injection level goes well beyond 10^{17} cm^{-3}), due to a strongly enhanced Auger recombination. For the D1 efficiency versus injection level, the situation is more complex. The SRH mechanism cannot be applied for extended defects [20]. The occupancy of the dislocation states may either gradually saturate at higher injection levels or show a field dependence.

The estimated internal efficiencies of the BB EL at a forward current of 50 mA are shown in Fig. 8 for all diodes. It can be seen that, in the case of B-implanted samples, the presence of dislocation loops leads to a suppression of the BB luminescence. The dislocation loops are formed during annealing, but will dissolve again when annealed at higher annealing temperature. The B-implanted samples annealed at 850 °C are therefore expected to have the highest dislocation loop density [21]. All samples then show that the BB luminescence decreases with increasing dislocation loop concentration.

D. Temperature Dependence of Luminescence

The competitive recombination through dislocation levels and via the BB transition also affects the temperature behavior of the EL. EL spectra recorded at various temperatures from the double-silicon-implanted sample are presented in Fig. 9 (top). As shown in the figure, the low-temperature spectra ($T < 100$ K) exhibit a well-pronounced D-band structure, with clearly distinguishable D1, D2, and D3 peaks (compare with Fig. 1). The peaks change shape, intensity, and position as a function of temperature. Data related to the changes in the integrated intensities of the D-band and BB peak and those related to the positions of their maximal intensities are presented in Fig. 9 (bottom).

As shown in Fig. 9, the BB-peak intensity increases substantially starting from $T > 180$ K, being under the detection limit at lower temperature. Such an increase in intensity of the BB peak with temperature correlates with that reported previously for P- and B-implanted Si samples [5], [7], [22], and is opposite to the temperature behavior of the BB peak in nonimplanted Si samples [5], [23]. At the same time, a decrease in the integrated intensity of the D-band was observed. Since the intensity of the BB peak in Si-double implanted samples at 300 K is still

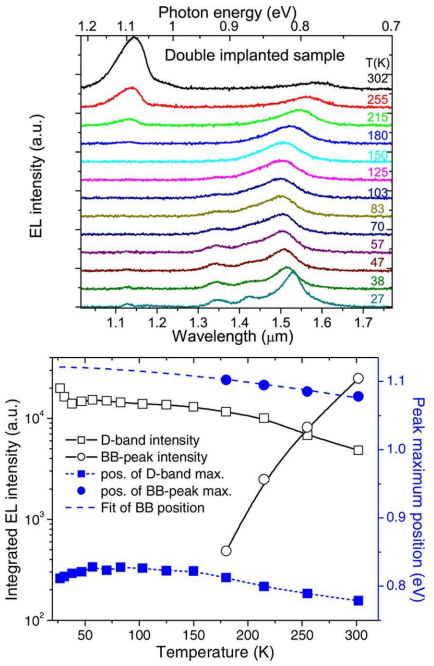

Fig. 9. Top: The EL spectra of a B-diffused double Si-implanted sample at various measurement temperatures. The forward current during the measurements was 20 mA. The curves are shifted in the vertical direction for clarity. In the spectrum detected at 27 K, the D1, D2, and D3 peaks are clearly distinguishable (cf. Fig. 1). Bottom: The signal intensities and positions of maximum intensity, derived from the upper figure. The dashed line shows a fit of the temperature dependence of the BB peak position following the study in [24]. The other lines are drawn to guide the eye.

$\sim$10 times less than that in nonimplanted ones, we suppose that the anomalous behavior of its intensity is related to redistribution of recombination processes between the BB recombination and the radiative and nonradiative recombination processes related to dislocations. Moreover, comparison of the changing ratios of the signal intensities in Fig. 9 (bottom) leads us to suggest that a substantial part of the dislocation-related recombination processes in the samples are nonradiative. PL from the D-band in the Si-implanted samples was detected at temperatures below 200 K. Similar to EL, the PL intensity of the D-band increased on the order of 200-keV implant $\rightarrow$ 450-keV implant $\rightarrow$ double implant.

The temperature dependence for the position of the maximum intensity of the BB peak corresponds to the expected dependence [24], as illustrated by the fit in Fig. 9 (bottom). The T-dependence for the D-band maximum position is more complex. A similar dependence for the D1 peak, which is reported previously [25], was attributed to the origin of D1 luminescence, i.e., to the radiative transition between two shallow levels related to dislocations.

The emission at 1.1 μm is strong at room temperature and above, as earlier reported in [2], [7], [9], and [22].

Room-temperature emission at 1.5 μm is considerably weaker in all our experiments. To determine the best method for the introduction of dislocations into silicon for 1.5-μm LEDs, including plastic deformation [8], wafer direct bonding [10], and ion implantation, further investigations are necessary.

IV. Conclusion

The impact of dislocation loops on the infrared light emission from silicon LEDs was studied. Silicon p^+n diodes were fabricated using boron diffusion, boron and silicon implantation, and thermal anneals. The resulting diodes show a strong variation in the density and physical location of implantation-originated dislocation loops—confirmed by TEM and HRXRD measurements. Strong light emission is observed around the BB recombination wavelength of 1150 nm, which is identified as phonon-assisted radiative recombination. The BB radiation becomes progressively weaker at lower temperature and with increasing dislocation loop density.

D-band luminescence shows the opposite trend, both in temperature and the dislocation loop density. From the found dependences, it is concluded that, with the applied manufacturing techniques (B diffusion, and B and Si implantation), the most efficient room-temperature silicon LED is formed by causing minimum lattice damage, emitting at the BB edge (1150 nm).

Ion-implanted silicon LEDs may present interest for light emission at 1.5 μm; however, to that purpose, the dislocation loop density must be strongly increased compared to the devices presented here, while nonradiative recombination processes must remain suppressed.

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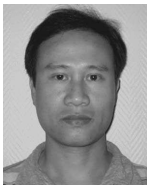

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Dr. Kittler acts as an Organizer of international conference series in the field of semiconductor materials research.

Chapter 6

Silicon-On-Insulator LEDs

Abstract

Silicon-On-Insulator (SOI) technology has in some fields of IC fabrication significant advantages over conventional bulk silicon technology and has received considerable investigations around the world. However, for application in LEDs, SOI LEDs suffer from poor EL efficiency compared to their bulk-Si counterparts. We realize that this low efficiency could be caused by the relatively large non-radiative recombination rate at the n^+ and p^+ contacts and at the Si/SiO_2 interfaces. In order to improve the radiative recombination, we did a series of experiments for realization and characterization of Si LEDs using SOI technology by means of reduction of the aforementioned non-radiative mechanisms.

The fabricated $p^+/p/n^+$ devices exhibited an external quantum efficiency of 1.4×10^{-4} at room temperature, with a spectrum peaking at 1130 nm, which is almost two orders higher than reported thus far for SOI LEDs. This large improvement is due to three confinement mechanisms, termed: geometrical effects, quantum-size effects, and electrical field effects. The structure utilizes two very thin silicon slabs close to the p^+/p and n^+/p junction to reduce the p^+ and n^+ contact area and to confine the injected carriers in the central lowly doped p-region. The field effects are implemented by administering the appropriate voltage at the poly-gates on top of the thin silicon layers and by controlling the voltage applied to the central poly-gate covering the p-region. With this approach, we realized an efficient compact infrared light source with high potential switching speed for on-chip integration.

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Introduction

The recent progress in silicon light-emitting diodes has led to power conversion efficiencies of 1 % (internal quantum efficiencies around 3 %), potentially offering a new integration approach for VLSI circuits with optical communication [1]. It was found that high-purity silicon with low doping levels and low defect density leads to the highest efficiency at the band-to-band recombination wavelength [2][3]. However, these high efficiency silicon LEDs emit infrared light from an extended volume. This lack of spatial confinement prohibits the formation of compact optical integrated structures, limits switching speed, and will lead to undesired cross-talk problems in integrated microsystems. One approach to a better confinement of the light emission is to form a silicon-LED in silicon-on-insulator (SOI) material. The fabrication of a lateral LED in thin-film high-quality SOI material has a few advantages over bulk silicon, such as higher optical switching speed with lower power consumption; better options for integration and coupling of the light into waveguides [4]. The full dielectric isolation of the active device layer forces confinement of the electrons and holes which increases the probability for light emission. These made this approach attractive, because both VLSI electronics and integrated optics are commonly fabricated on SOI wafers [5]. Yet, the highest reported efficiency of silicon LEDs on SOI is two orders of magnitude lower than in bulk silicon LEDs [6].

As discussed in Chapter 2, the emission efficiency can be improved significantly in a lateral light emitting diode realized on high-quality SOI wafers, as long as the non-radiative recombination processes occurring mostly at the interfaces [7][8] and at the p^+ and n^+ contact [9] are well suppressed. We realized that by locally tailoring the thickness of the silicon layer towards nanoscale dimensions (< 10 nm) at positions close to the p^+/p and n^+/p junction of the p^+/p/n^+ structure. The fabricated devices exhibit a high quantum efficiency for SOI-LEDs, closing in on bulk silicon efficiency levels. They were manufactured with normal VLSI processing procedures.

With this chapter, in the *Approaches* section we introduce novel device structures that reduce the non-radiative recombination by confining the carriers in an SOI peninsula and by redistributing carrier concentration at the interfaces through field effects. The SOI peninsula is connected to p^+ and n^+ regions by thin slabs making it possible to further enhance the carrier confinement. In order to create very thin SOI layers we used the well-known self-limiting oxidation mechanism [10][11] where the oxidation rate retards when the Si layer approaches nanoscale dimensions due to strain introduced in the thin Si films. This phenomenon helps us in getting a better uniformity of the thin film. The SOI film was reduced to the final thickness by the layer-to-layer oxidation technique [12] which will be presented in the *Experimental* section. In the next section, measurements of ox-

ide quality and carrier lifetime are introduced. Followed by the characterization data of electrical and electroluminescence properties obtained from the fabricated devices with supporting results from device simulation.

6.1 Approaches

In order to realize an efficient light emitting diode on SOI materials, two approaches were proposed and carried out in our research. With these two approaches we limit the non-radiative recombination probability at the interfaces and at the contacts, and consequently the radiative recombination is enhanced.

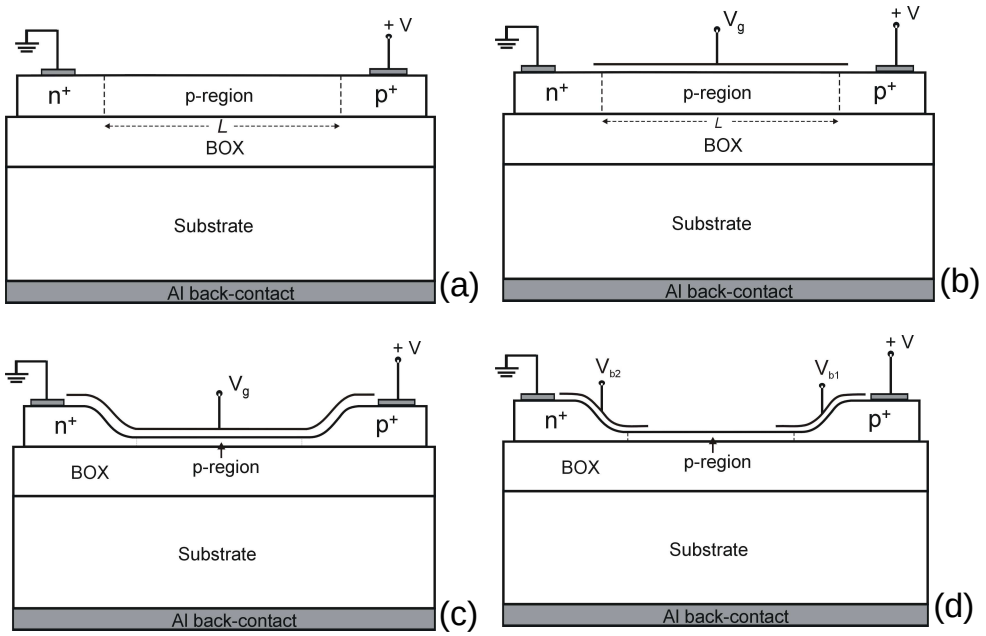


Figure 6.1: Cross-section drawing of the lateral $p^+/p/n^+$ diode with four variations of the p-region.

The first approach is a lateral $p^+/p/n^+$ diode structure with four variations of the p-region: normal or thinned p-region and with or without poly-gate on the central region (see Figure 6.1a, 6.1b, 6.1c, 6.1d). Comparison of EL intensity from structure 1a to that of structure 1b offers the ability to study the influence of interface recombination. Structure 1c and 1d enables to investigate the band-gap widening effect performance when the central emitting region is scaled down to less than 10 nm thick. The silicon band-gap energy will increase significantly [13] [14]; therefore, when electrons and holes are injected into this thinned region, they will recombine and emit light with shorter wavelength corresponding

to its widened band-gap. Applying a suitable voltage to each poly-gate covering the two ends of the thinned p-layer presented in Figure 6.1d helps to enhance the injection process of electrons and holes into the central emitting region.

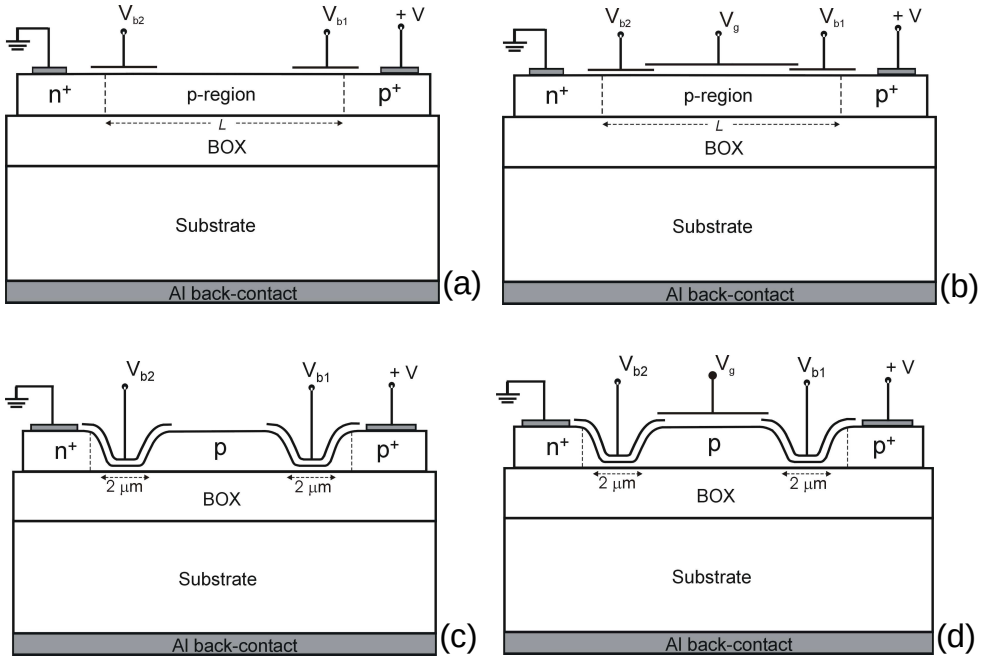


Figure 6.2: Schematic structure cross-section of lateral $p^+/p/n^+$ LEDs with two gated access regions: (a)/(b) no thinning and without/with central gate; (c)/(d) thinned down and without/with central gate.

In the second approach, we introduce new structures of $p^+/p/n^+$ diodes, in which electrons and holes are injected into the central volume through a gated access-layer (see Figure 6.2). By doing this the non-radiative recombination at the p^+/p and n^+/p junction can be strongly suppressed due to three subsequent mechanisms. Firstly, by administering the appropriate voltage at this poly-gate, minority carriers face a potential barrier during the way out when trying to escape from recombination within the active region. Secondly, by locally thinning down the access-layer, electrons and holes after being injected into the central region have difficulty to find out the exit through diffusion. Finally, as the silicon layer was scaled down to less than 10 nm thick, the band-gap widening effects may play a role to further increase the confinement. With this approach, after being injected into the central area electrons and holes will have more probability to recombine there and have less chance to reach the contacts. As a result the emission efficiency was strongly enhanced. Moreover, the non-radiative interface recombination can be controlled by electric fields for additional improvement, see

Figure 6.2b and 6.2d. Part of the results were presented in [15].

The two series of SOI $p^+/p/n^+$ LEDs with different sizes can all be realized in the same processing procedure. In the following parts, all optical and electrical characteristics obtained from them will be presented subsequently.

6.2 Experimental

6.2.1 $p^+/p/n^+$ diode realization

All devices corresponding to the aforementioned approaches were realized on the same wafer and under the same fabrication conditions. The thickness variation of the thinned down layer was carried out on four quadrants by defining the wafer into four parts. In this way we expect that when comparing a diode with the same structure on one wafer-part to that on others the unwanted variations can be ignored. A general process-flow used for realization of includes:

1. *SOI island formation*. The starting material is a 100 mm p-type "Smart-Cut" substrate with a silicon device layer of 150 $\pm$ 2 nm on top of a buried-oxide (BOX) layer of 400 nm. The device layer is B-doped silicon with a resistivity of 1-10 Ωcm. After thermal oxide growth, the device layer is selectively etched into different islands with desired sizes by wet etching in TMAH 10 % solution at 50 °C. In these SOI islands the devices with different structures were realized.

2. *SOI thinning*. A standard local oxidation of silicon (LOCOS) technology was used step by step to locally create the very thin regions at the desired positions. After each oxidation step, the grown-oxide was checked for its thickness by ellipsometry and then removed by buffered-HF. In order to examine the remaining thickness of the SOI layer, the step-height was measured with a DekTak (Veeco DekTak 8).

3. *Gate-oxide growth*. After the thinning process, the Si_3N_4 layer was removed by immersing the whole wafer in H_3PO_4 85 % solution at 150 °C for 15 minutes. A final 12 nm gate-oxide was grown at 900 °C in a dry-oxygen ambient.

4. *p^+ and n^+ formation*. The highly doped p^+ and n^+ regions were formed by ion implantation with BF_2^+ and As^+ respectively, with a dose of 5×10^{15} ions/cm^2. Dopants were activated by furnace anneal in a nitrogen environment at 800 °C for 30 minutes.

5. *Deposition of first poly-silicon.* A 300 nm LPCVD poly-Si layer was doped by implantation with Phosphorous at a dose of 1×10^{16} ions/cm^2, and then patterned. This forms a poly-gate on top of the thinned regions.

6. *Deposition of gate-oxide at the central p region.* To insulate the first poly-gate from the central gate a 30 nm thick oxide layer was deposited at 800 °C by LPCVD, followed by a strengthening step of the deposited oxide by annealing in nitrogen ambient at 900 °C for 30 minutes. Then the gate oxide layer covering the central p-region includes two layers: 12 nm thermally grown oxide and 30 nm LPCVD oxide.

7. *Deposition of second poly-silicon.* The poly-silicon gate covering the central active region was formed similar to the first poly-silicon layer.

8. *Contact and passivation.* Metal contact areas were fabricated by sputtering of a Ti/W barrier layer and Al (+1 % Si) on the wafer after opening the contact windows. Finally, the Si/SiO_2 interface was passivated by treatment in wet nitrogen at 400 °C for 10 minutes.

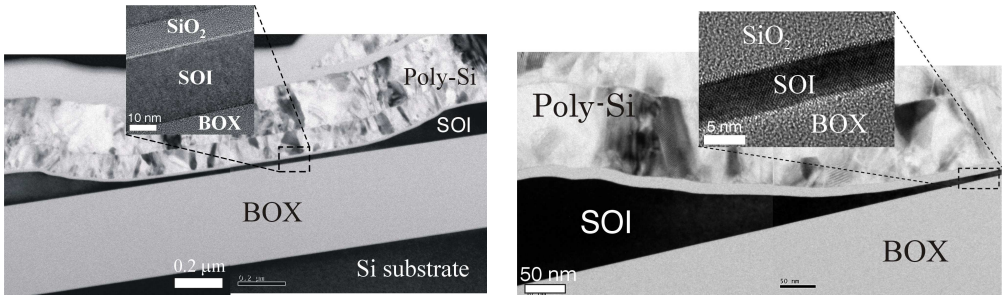
The fabricated devices have not yet received any special treatment, like surface texturing or anti-reflection layer covering, for enhancing the outcoupling of light.

6.2.2 Profile of thinned-down SOI layers

The cross-section of the thinned SOI layers was analyzed by the HR-TEM. Four cross-section TEM specimens corresponding to four thickness variations were processed by the focus ion beam (FIB) technique. The thickness of these four thinned layers can be observed from their HR-TEM images, and were found to be 27 nm, 19 nm, 10 nm and 5 nm thick. This value has an uncertainty of $\pm$ 2 nm across the wafer because of the initial SOI uniformity. All HR-TEM images present a very uniform profile of SOI thin-film as well as a very good Si/SiO_2 interface. Uniformity within a single thinned SOI layer is estimated of 0.5 nm. As an example, HR-TEM images of 27 nm and 5 nm layers are shown in Figure 6.3a and 6.3b respectively.

6.2.3 Electroluminescence measurement setup

All electroluminescence (EL) measurements from these device series were carried out with the infrared camera system via the microscope at various magnifications (see chapter 3). The emission spectrum of the LED was extracted at a randomly chosen position on the emitting area from the obtained image. The integrated EL intensity was collected from the image.



(a) 27 nm SOI (b) 5 nm SOI

Figure 6.3: Bright field cross-section HRTEM image of: (a) 27 nm thinned SOI layer; (b) 5 nm thinned SOI layer.

6.3 Gate oxide and interface quality

6.3.1 C-V measurement

The gate oxide quality was examined by C-V measurements. Four series of MOSFET test-structures were realized respectively for the first poly silicon (covering the thinned regions) and the second poly-silicon (covering the central p region) in the same fabrication process as the $p^+/p/n^+$ diodes on the same SOI wafer. Figure 6.4 shows an example of the n-type MOSFET cross-section and also the measurement setups. In this measurement the source, drain and substrate were grounded. The capacitance was measured between the front gate electrode and the three others.

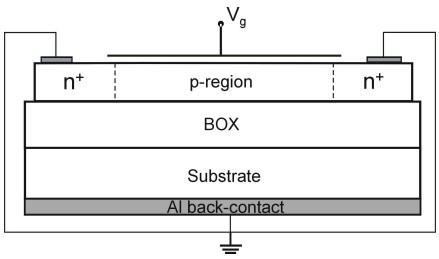


Figure 6.4: Cross-section of n-type MOSFET test structure and the C-V measurement setups.

The high frequency C-V characteristics of these four MOSFETs were measured at 100 kHz frequency and are presented in Figure 6.5. From the measured C-V characteristics, according to MOSFET theory (example in [16]) we can say that our formed gate-oxide is of high quality. The capacitance formed by the second poly-gate is approximately 4 times lower than that of the first one because

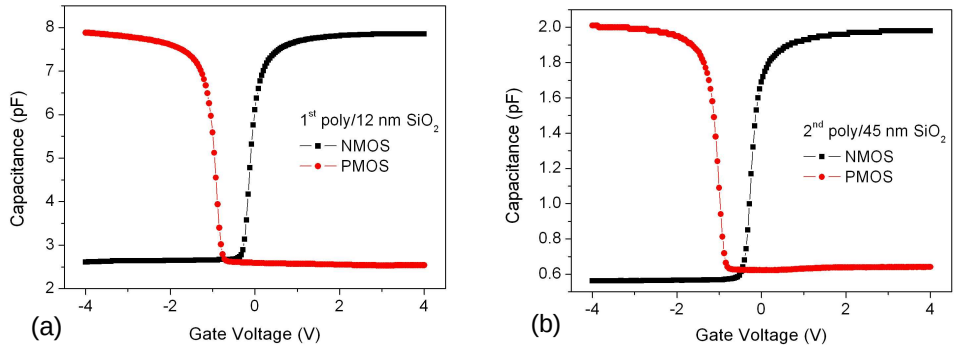


Figure 6.5: High frequency C-V Characteristics of n-MOS and p-MOS structures measured at 100 kHz for: (a) the first poly; and (b) the second poly.

of an almost 4 times thinner oxide-gate compared to the second one. These C-V curves also indicate a low fixed interface charge concentration. This once more confirmed that the SOI islands are bounded by a high quality thermally grown oxide. Moreover, we can also extract threshold voltage of the MOSFET from these C-V curves. The threshold voltage of the n-MOS for both gate-oxide layers is approximately -0.2 V, whereas for the p-MOS it is about -0.9 V. Note that the poly-gates are n-type doped for both channel types.

6.3.2 Carrier lifetime measurement

The interface quality is an important issue especially for SOI devices. If we are able to quantitatively obtain the portion of the interface recombination rate over the total recombination, we will know how the interface recombination affects the carrier recombination lifetime in a semiconductor device. In the following paragraph we deal with the recombination in the volume of the SOI layer and at the top- and bottom oxide-silicon interface. The test structure and measurement setup are presented in Figure 6.6. We follow the method described in [16] and [17]

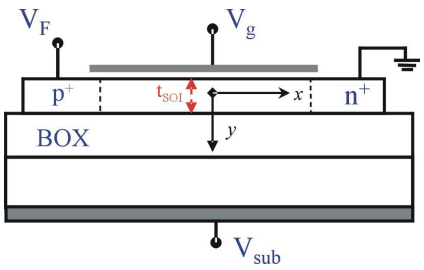


Figure 6.6: Cross-section drawing of a gated p-i-n diode used for extraction of the lifetime recombination at Si/SiO_2 interfaces and within silicon volumes.

with the following assumptions: we assume that the energy level of the effective recombination centers in the volume and at the oxide interfaces of the SOI layer are at mid-gap. This assumption does not mean that the origin of these traps is the same. The interface-traps could be Si dangling bonds whereas the volume traps are e.g. due to metal contamination.

We further assume that recombination lifetime of electrons and holes in the volume (τ_{n} and τ_{p} respectively) are the same. This means that according to the equation

$$\tau = \frac{1}{(\sigma_{\mathrm{v}} \upsilon_{\mathrm{th}} N_{\mathrm{tv}})} \tag{6.1}$$

the product of σ_{v}, the capture cross section of traps in the SOI volume and υ_{th}, the thermal velocity of the carriers are the same, $\mathrm{N_{tv}}$ represents the trap-density per cm^3.

For the interface recombination we make similar assumptions and

$$\mathrm{s} = \frac{1}{(\sigma_{\mathrm{s}} \upsilon_{\mathrm{th}} \mathrm{N_{ts}})} \tag{6.2}$$

where s is the surface recombination velocity and $\mathrm{N_{ts}}$ is the surface density of interface traps per cm^2. We further assume that when the electric field due the top gate and bottom gate is at the same level, the potential distribution in the silicon is flat. This assumption holds for doping levels of $< 10^{16}$ ions/cm^3 which is the case in our samples. For such low doping levels in the p-region also band-gap narrowing can be ignored. We will now derive equations for the volume and surface recombination and we do so under the condition of very low injection level. Under this condition the potential along the x direction is flat and potential drops occur across the n^+/p junction and across the p/p^+ junction. Calculations based on the assumptions above make the results semi-quantitative but we are looking after trends and orders of magnitude rather than an outcome with high precision.

The SRH theory results into the following equations for volume and surface recombination:

$$R_{\mathrm{v}} = \frac{1}{\tau} \frac{\mathrm{n\,p} - \mathrm{n_i^2}}{\mathrm{n + p + 2n_i}} \qquad \text{and} \qquad \mathrm{R_s} = \frac{\mathrm{s} \cdot (\mathrm{n_s\,p_s} - \mathrm{n_i^2})}{\mathrm{n_s + p_s + 2n_i}} \tag{6.3}$$

where n and p are electron and hole concentration distributions across the silicon film respectively. They are related to the intrinsic carrier concentration, $\mathrm{n_i}$, as

$$\mathrm{n\,p} = \mathrm{n_i^2}\ \exp\left(\frac{\mathrm{qV_F}}{\mathrm{kT}}\right) \tag{6.4}$$

with q is the elementary charge, $\mathrm{V_F}$ is the forward-bias voltage, and *kT* is the thermal energy.

The maximum recombination rate in the SOI film and at the interface can be calculated from $\partial R(\mathrm{n})/\partial \mathrm{n} = 0$, and which is found for the condition n = p. The maximum volume and surface recombination are now given by

$$R_{\mathrm{v\,max}} \cong \frac{1}{2\tau}\mathrm{n_i}\exp\left(\frac{\mathrm{qV_F}}{2\mathrm{kT}}\right) \tag{6.5}$$

and

$$R_{\mathrm{s\,max}} \cong \frac{\mathrm{s}}{2}\mathrm{n_i}\exp\left(\frac{\mathrm{qV_F}}{2\mathrm{kT}}\right). \tag{6.6}$$

The condition of n = p in the lowly doped region will now be achieved under certain conditions for the gate bias on the bottom and top gate.

In fact, at the Si/SiO_2 interfaces in the SOI structures, the concentration of electrons and holes can be equal only when it is in depletion condition, i.e., the front- (or back-) interface recombination rate reaches a maximum when it is put at depletion. However, due to interface coupling effects the peak current position changes correspondingly to each bias voltage at the opposite gate. Whereas, recombination occurring within the thin-film SOI volume shows a maximum when the front-gate and back-gate are biased in such a way that the potential and carrier concentration profiles in the SOI film are nearly flat. At this condition, the recombination rate is constant in the whole p-region volume; therefore, the maximum recombination current in the SOI film can be simply equal to the product of the maximum volume recombination rate ($\mathrm{R_{v\,max}}$) and the p region volume:

$$I_{\mathrm{v\,max}} = q\,R_{\mathrm{v\,max}}\,(t_{\mathrm{SOI}}\,W\,L) \tag{6.7}$$

where $\mathrm{t_{SOI}}$, W and L respectively are the thickness, width and length of the p-region. And similar for the maximum recombination current at the Si/SiO_2 interface, we have

$$I_{\mathrm{s\,max}} = q\,R_{\mathrm{s\,max}}A_{\mathrm{interface}} = q\,R_{\mathrm{s\,max}}\,(W\,L)\,. \tag{6.8}$$

Figure 6.7 shows the diode current $\mathrm{I_D}$ through a gated $\mathrm{p^+/p/n^+}$ diode with the p region of 146 nm thick, 5 μm long, and 60 μm wide at a forward-bias $\mathrm{V_F}$ = 0.3 V when scanning the front-gate voltage ($\mathrm{V_{fg}}$) from -3 V to +3 V, whereas the back-gate voltage ($\mathrm{V_{bg}}$) was chosen in the range of -20 V to +20 V. Since the buried oxide is much thicker than the front gate oxide, in order to get comparable fields we need higher voltages at the back-gate.

The current peaks in the middle of the figures show the overall recombination current, when the front and back interface are depleted together. All three current components, i.e., recombination current at the front- and back-interface as well as

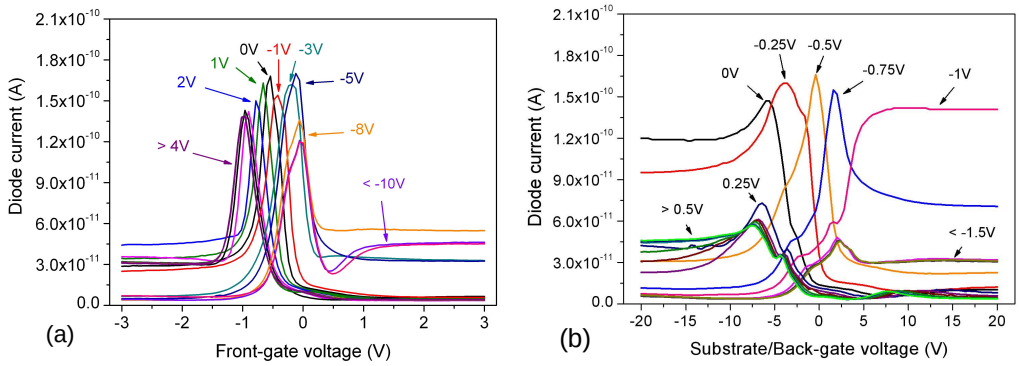


Figure 6.7: Forward current of a lateral $p^+/p/n^+$ diode (146 nm thick, 5 μm long, and 60 μm wide) at V_F = 300 mV as a function of: (a) front-gate bias at different back-gate voltages; (b) back-gate voltage at different front-gate levels.

recombination in the bulk of the thin film, are active and we can use this peak value (I_{max}) to calculate the effective recombination lifetime, τ_{eff}, from the equation

$$\tau_{eff} = \frac{q\, n_i\, t_{SOI}\, W\, L}{I_{max}} \exp\left(\frac{qV_F}{2kT}\right) \tag{6.9}$$

with τ_{eff} is related to the surface recombination velocity at front (s_f) and back (s_b) interfaces by formula

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_v} + \frac{s_f}{t_{SOI}} + \frac{s_b}{t_{SOI}}. \tag{6.10}$$

When the front interface is strongly accumulated and the back interface is strongly inverted (i.e., $V_{fg} <$ -1.5 V and $V_{bg} >$ 4 V), or vice versa (i.e., $V_{fg} >$ 0.5 V and $V_{bg} <$ -10 V), the current is saturated as a plateau (see Figure 6.7). The volume recombination component is only contributing to this saturated current. Under this condition, recombination is only effective in the central region of the SOI film, where electron and hole concentrations are stably equal. If we assume a linear potential distribution across the SOI film thickness, the recombination current in this film can be given by

$$I_v = f_c\, q\, R_{max}\, (t_{eff}\, W\, L) \tag{6.11}$$

where t_{eff} is the effective film thickness, f_c is a correction factor for the case when one assumes no band-gap narrowing effect and linear potential distribution across the SOI film thickness. Since these assumptions are reasonable for our diode at the chosen working conditions, the correction factor in this case is approximately equal to 1. From now we will skip f_c in our calculation.

According to [17] one can obtain t_{eff} from the equation:

$$t_{eff} = t_{SOI} \frac{2kT/q}{|2\phi_F - V_F|} \tag{6.12}$$

where $\phi_{\mathrm{F}} = (kT/q)\ln(\frac{\mathrm{N_A}}{\mathrm{n_i}})$ is the Fermi potential of the p region with doping concentration of $\mathrm{N_A} = 1 \times 10^{16}$ /cm^3. We have $\mathrm{t_{eff}} = 25.6$ nm. It is now possible to extract the volume recombination lifetime, τ_{v}, from

$$I_{\mathrm{plateau}} = \frac{q\, t_{\mathrm{eff}}\, W\, L}{\tau_{\mathrm{v}}} \mathrm{n_i} \exp\left(\frac{\mathrm{qV_F}}{\mathrm{2kT}}\right) \tag{6.13}$$

Taking the plateau current of 32 pA from Figure 6.7b, the volume recombination lifetime (τ_{v}) obtained from Eq. (6.12) and (6.13) is 1.3 μs.

In Figure 6.7a, when the back interface is inverted ($\mathrm{V_{bg}} > +4$ V), we see current peaks at a constant front-gate voltage (-1 V), this is confirmed by the plateau current belonging to a front-gate voltage of -1 V on Figure 6.7b. This current is the sum of the front interface and the volume recombination components. Therefore, it is easy to obtain the front interface recombination current from Figure 6.7b.

When both interfaces are driven to either strongly inverted or accumulated, at subthreshold region (small forward bias) we see almost no current flowing through the devices (very low plateau). That is because at this condition we indeed have a narrow base device but the carriers can not pass through the narrow base to reach the opposite carriers for recombination due to high repelling fields.

When assuming a uniform trap distribution in the Si/SiO_2 interface, the front interface current can be expressed using (6.6), as

$$I_{\mathrm{front}} = q\, R_{\mathrm{sf\,max}} W\, L = q\, \mathrm{s_f\, W\, L\, n_i} \exp\left(\frac{\mathrm{qV_F}}{\mathrm{2kT}}\right) \tag{6.14}$$

and a value of 6 cm/s was calculated for the front interface recombination rate.

Similar for the back-gate interface, we obtained a back interface recombination rate of 1 cm/s (the same level as in [17]).

To analyze the influence of the active region length (p-region) on recombination fraction between the volume and interface components, we do the same measurements on two other diodes having the p region with the same width and thickness but the length of 20 μm and 60 μm. The results are presented in table 6.1:

Length of the p-region (L)	5 μm	20 μm	60 μm
Volume recombination lifetime (τ_{v})	1.3 μs	1.2 μs	1.4 μs
Front interface recombination velocity ($\mathrm{s_f}$)	6 cm/s	1.5 cm/s	0.3 cm/s
Back interface recombination velocity ($\mathrm{s_b}$)	1 cm/s	0.5 cm/s	0.5 cm/s

Table 6.1: Recombination parameters in the silicon volume and at the interfaces of SOI $p^+/p/n^+$ diodes with different lengths extracted experimentally at low injection level.

These data show that the interface recombination current decreases when increasing the device length. When the length increases from 5 μm to 60 μm, the decrease of s_f and s_b is because of two reasons: decrease of injection level for a longer device since we measured at the same forward bias voltage (0.3 V); less effects of n^+ and p^+ contact recombination (see chapter 2 for more information) for a longer device. This also indicates that the fraction of radiative recombination within silicon volume over the non-radiative recombination at the interfaces was improved for a longer device; therefore, it may emit more light compared to a shorter diode at the same injection level. That relation will be examined by electroluminescence measurements of this device series.

From the obtained volume recombination lifetime of $\sim$1.3 μs, we can by using Eq. (6.1) estimate a trap density $N_t = 10^{14}$ /cm^3. This is a rather high value compared to the high quality bulk silicon nowadays where $N_t = 10^{10}$ /cm^3 is typical. However, this high value can be explained if we assume that during the fabrication process an amount of 2×10^9 /cm^2 contaminating atoms was introduced. This contamination level is not very unlikely for the standard VLSI technology and at the detection limit of TXRF (Total Reflection X-Ray Fluorescence). For bulk silicon material (500 μm thick) it remains actually a very low value when such an amount of contaminants diffuse into the bulk while for a 200 nm thick SOI layer it results into a high volume concentration. This can be seen as a realistic problem for the SOI technology in general and requires ultra clean chemicals and procedures as well as detection techniques in order to master the contamination level.

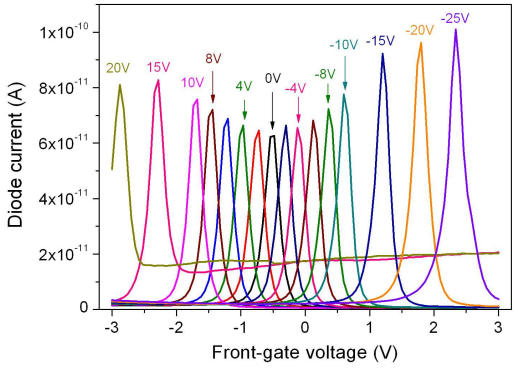


Figure 6.8: Forward current of a thinned $p^+/p/n^+$ diode (5 μm x 60 μm x 27 nm of p-region) at V_F = 300 mV as function of front-gate bias at different back-gate voltages.

This measurement was also carried out on the diode with a thinned active region, and the information given from these measurements was insufficient to enable to extract each recombination component. An example for diode with a 27 nm thick p-region is presented in Figure 6.8. We see that the current peak

position depends on the applied voltages at the opposite gate. Since we could not identify any characteristics from the volume current while the measured data only relatively indicated the profile from interface recombination components, we are just able to say that the interface recombination dominates over the volume component in this type of device. It means that a thicker SOI layer is preferred for lateral light emitting diode realizations.

The lifetime measurements presented above are only indicative in order to give us an idea for the trend of the relative carrier recombination distribution in a SOI LED because in fact our LEDs normally work at higher injection conditions, where the diffusion current dominates over the recombination current, thus the absolute carrier lifetime will be different from the obtained data.

6.4 Characterization of lateral $p^+/p/n^+$ diodes with different p-region dimensions

The realized $p^+/p/n^+$ diodes vary in the dimension of the emitting region: three width levels of 20, 40 and 60 μm and the length increases from 5 μm to 60 μm. The realized thinned regions as mentioned in the *Experimental* section were 146 nm (normal LED), 27 nm, 19 nm, 10 nm and 5 nm. In this section we only focus on the device structures in Figure 6.1, which were proposed above as the first approach.

6.4.1 Electrical properties

I-V characteristics of normal $p^+/p/n^+$ diodes (devices in Figure 6.1a) with different sizes of the p-region were analyzed and are exhibited in Figure 6.9. All of

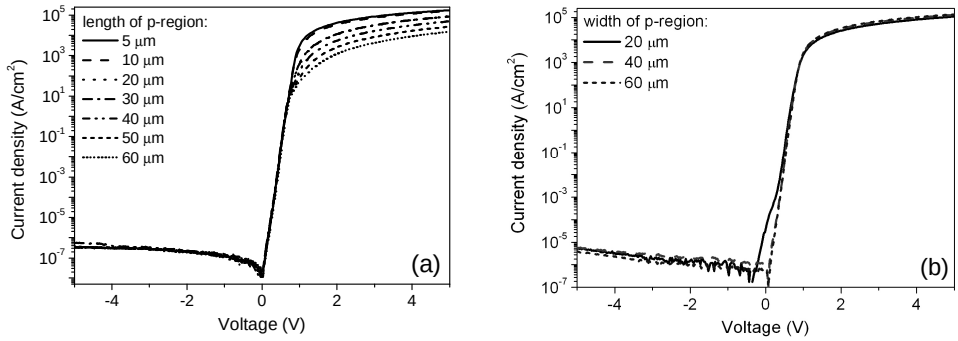


Figure 6.9: I-V characteristics of $p^+/p/n^+$ diodes depend on the length with the same width of 60 μm (a); and on the width at the same length of 20 μm (b).

them show a good diode profile, with a slope of 68 to 72 mV/decade at low injection regime depending on the p region dimensions. The series resistance increases when increasing the length and decreasing the width of the active volume.

The fabricated diode with different thickness was also characterized. The diode resistance increases significantly when reducing the Si film thickness. The *I-V* curves of five diodes with the same structure except p-region thickness (146–5 nm) are presented in Figure 6.10. Decreasing the p-region thickness from 146 nm to 5 nm, resulted in diode resistance increase of 10 times and the sub-threshold slope was also affected.

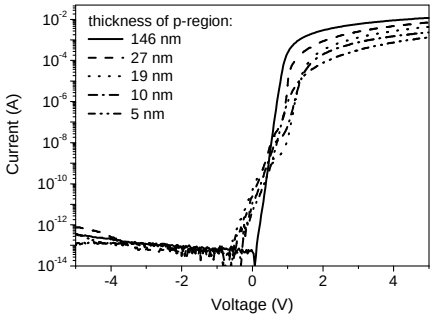


Figure 6.10: Diode I-V characteristic was affected by silicon film thickness. Five diodes have the same structure except the p-region thickness.

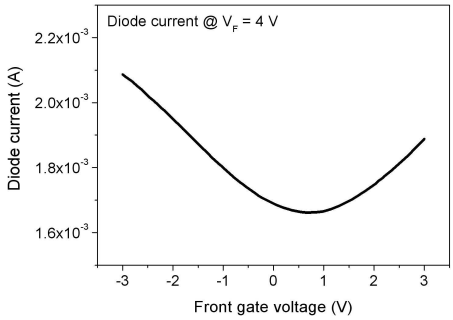


Figure 6.11: Diode current as function of front-gate voltage when applying a forward bias of 4 V. The diode is with p region dimensions of 20 μm x 60 μm x 146 nm.

The influence of the center gate-voltage is not the same as in CMOS. In our lateral diodes a corresponding current always flows from p^+ to n^+ electrode at a certain forward bias. With the structure shown in Figure 6.1b, the gate-voltage can be used to modify the diode current but cannot block it. A 20 μm long structure was examined at a constant forward bias (V_F = 4 V). The change of current when scanning the front gate voltage from -3 V to +3 V is shown in Figure 6.11. A higher diode current was observed when the front Si/SiO_2 interface was driven to accumulation or inversion since in both cases the carrier density in the channel under the poly-gate was enhanced and an extension of either the p^+ contact or n^+ contact was occurred under the gate. A minimum current was seen at a gate voltage of $\sim$0.6 V, when the silicon film was depleted. Note that here the diode was working at much higher injection level, where the diffusion current dominated over the recombination current. The diode behavior then is different compared to a low injection condition as was used in carrier-lifetime measurements.

6.4.2 Optical properties

We analyzed the electroluminescence characteristics of these diode series using the infrared camera system (XenICs). At room temperature, all diodes exhibit a band-to-band recombination peak at around 1130 nm. An example of the emission spectrum at a 5 mA current (corresponding current density of 5.7×10^4 A/cm^2) is shown in Figure 6.12. This EL profile indicated normal phonon-assisted

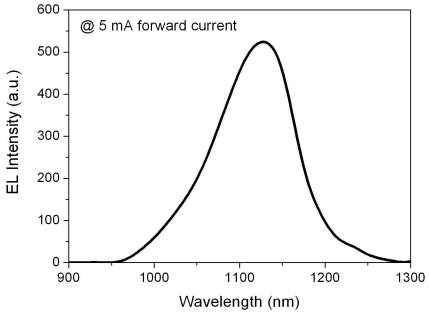


Figure 6.12: EL spectrum of a normal SOI diode with a 5 μm $\times$ 60 μm (L $\times$ W) of active region at a current density of 5.7×10^4 A/cm^2.

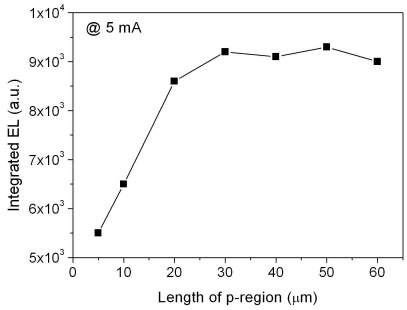


Figure 6.13: Integrated EL of a normal SOI diode as a function of device length at the same current density of 5.7×10^4 A/cm^2.

silicon band-edge recombination [6]. The influence of the integrated EL intensity on the device length is included in Figure 6.13. It shows that with the same width (60 μm) and thickness (146 nm) of the p region, EL intensity increased when the length rises from 5 μm to 20 μm and remains at almost the same level until 60 μm. It is qualitatively in agreement with carrier lifetime measurements presented above. According to our calculations presented in chapter 2, the non-radiative recombination at the p^+ and n^+ contacts have more influence on the device with a shorter length. For diodes with p-region longer than 20 μm, the effects of the contact recombination are almost at the same level.

We expected that a small shift of EL peak to a shorter wavelength would be observed after reduction of the thickness of p-regions below 10 nm, however, it could not be seen with our optical system because the optical signals were under the detection limit of our ImSpectro-Camera system while it was not possible to inject a sufficient high current through the very high resistance layer. There is a possibility to enhance conduction of this silicon thinned film by creating a conduction channel within that thinned film using a suitable voltage at the center poly-gate (structure on Figure 6.1c) or confine the injected carriers in the thinned film using electrical field effects created by the two poly-electrodes (structure on Figure 6.1d). But in spite of doing this, radiative recombination processes just take place mostly outside the thinned volume. This can be seen for example in

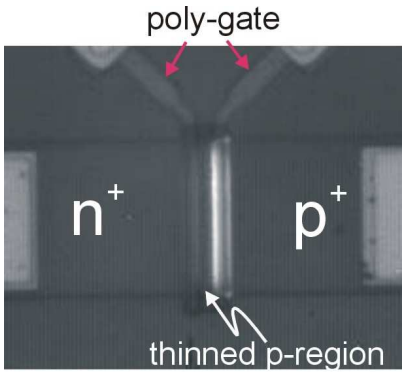


Figure 6.14: Top-view photograph of the thinned $p^+/p/n^+$ diode (structure 6.1d) at 1 mA forward current, taken by InGaAs camera via a 50x-microscope. The central p-region is 10 nm thick, 10 μm long, and 60 μm wide. The poly-gate close to the p^+/p junction was biased at -1 V and the poly-gate close to the n^+/p junction was at 1 V. The electrodes and SOI island were visible because of weak illumination from an external lamp.

Figure 6.14: we see the light emitted mostly at the p^+ side, very weak light emitted from the n^+ side, and no emitted light from the central thinned region.

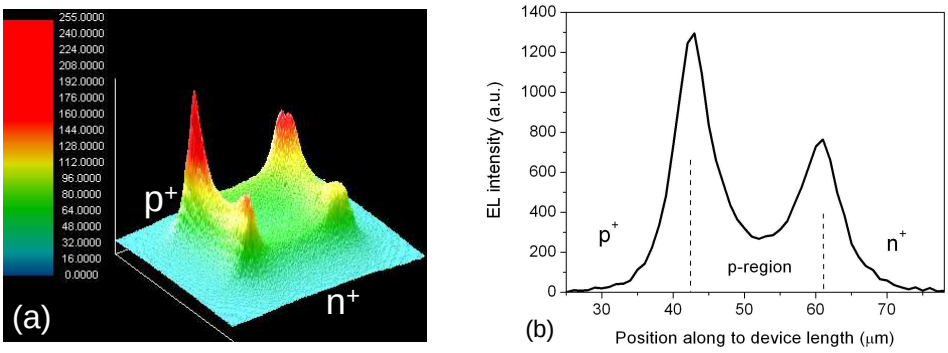


Figure 6.15: Far-field view of the light emitting profile from a normal $p^+/p/n^+$ diode. (a) 3D view of the emitting area (20×20 μm^2 of p-region): front-right is n^+ region; the opposite is p^+ region. We can see a higher emitted light intensity at device edges and at the junctions. (b) Light intensity as a function of position along the device length across the p-region.

In a far-field view of the electroluminescence profile, Figure 6.15 shows the top-view photograph of the emitting area taken by the CCD camera*. We see that the light intensity is higher at the edge of the silicon film compared to the central

*This measurement was done with a VIS-AR coated CCD camera at Philips Research, Eindhoven, by Victor Zieren and Martijn Goossens.

region because of wave-guide effects of the emitted light inside the silicon layer. Since the emitted wavelength is in the same range of the product of thickness and silicon refractive-index, the light after being generated is partly confined within the silicon slide and escapes at the silicon edge. It is also easy to recognize that the light peak generated at the p^+/p junction is higher than that at the n^+/p junction. The light intensity profile along the device length is proportional with the product of electron and hole concentration. At high injection level for a lateral p^+/p/n^+ diode, the number of electrons and holes are equal within the central p-region and are more dominant at the p^+/p junction compared to that at the n^+/p junction. This can be explained entirely by the p-i-n model presented in [7, 18, 19], in which the most effective issue was that electrons are more mobile than holes at the same injection condition.

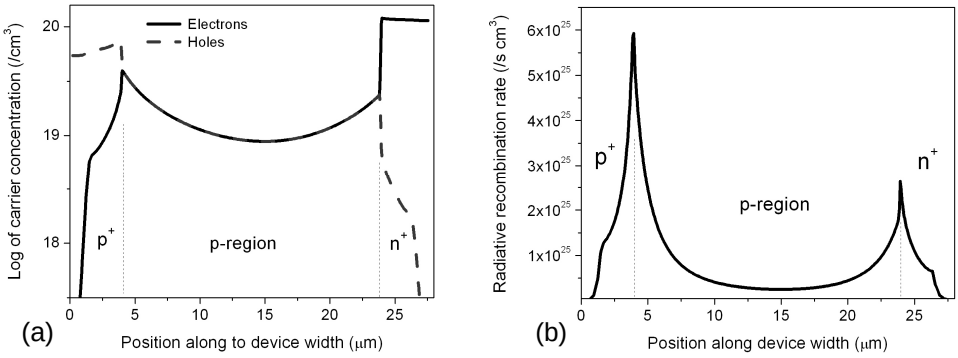


Figure 6.16: Atlas simulation data for a p^+/p/n^+ structure under high injection condition: (a) electron and hole concentration as function of position along a cut-line from p^+ to n^+ region; (b) band-to-band radiative recombination profile belonging to this carrier distribution. Band-gap narrowing was not taken into account in this simulation.

Distribution of carrier concentration and radiative recombination along the device-length was modeled with the Atlas simulator of Silvaco. The simulated data included in Figure 6.16, essentially support the experimental observations.

Self heating effects of SOI materials give an additional influence on the device efficiency. In SOI materials, a silicon thin-film is insulated not only electrically from the handle silicon wafer but also thermally by a thick buried-oxide layer, because of its low thermal conductivity. Working under a high current density produces heat, whereas the generated heat is not able to be released as fast as necessary. As a result, the device body becomes hot quickly. In our experiments, the critical current level is just in a range of a few tens of milliampere. As an example shown in Figure 6.17, a diode with a p-region of 20 μm long and 20 μm wide was blown up just after a few minutes at 45 mA forward current (current density of 1.13×10^6 A/cm^2). The blown-up area is close to the p^+/p junction

and under the aluminum layer, in which a higher recombination rate has taken place. The temperature distribution in the device body was simulated using the Atlas simulator and shows a good agreement with the experimental observations in Figure 6.18.

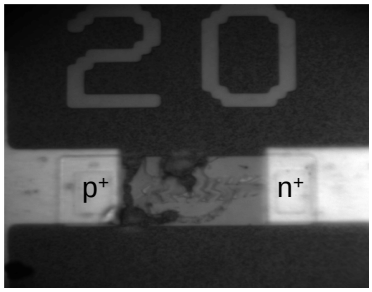


Figure 6.17: Top-view photograph of a failed diode after just a few minutes at 45 mA.

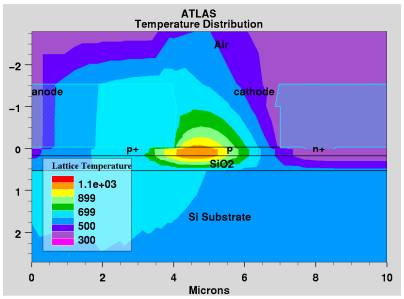


Figure 6.18: 2D simulation of temperature distribution inside a diode cross-section under high injection condition.

The *I-V* characteristic of the SOI diodes is also influenced by self-heating. Figure 6.19 exhibits a comparison of simulation data when the self-heating effects are taken and are not taken into account for the device-style presented in Figure 1a. The diode series resistance increases during operation because of a rise in temperature. Note that in 2-D simulation, the unit of current flowing through a device is calculated as A/μm, in other words, it is calculated for a device with 1 μm width.

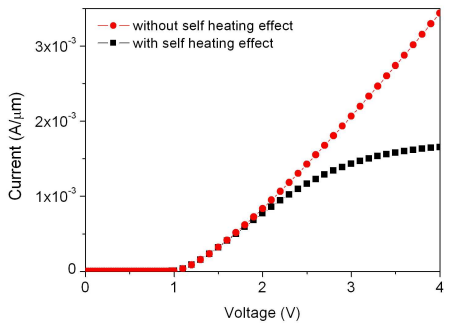


Figure 6.19: Simulation data of self heating effect on diode *I-V* characteristics.

The EL profile can be modified by applying a voltage to the front gate. When scanning the gate voltage from accumulation to inversion the light intensity peak at the two junctions can be strongly modified (see Figure 6.20a) and the change of light intensity peak at the n^+/p junction is larger than that at the opposite junction. It signifies that the gate voltage does not only have effects on the interface but

also on the junctions, and therefore the change of EL intensity will be the total effect of both components. However, responding to the voltage scanning the total integrated EL changed by only a few percentages depending on the injection level (Figure 6.20b).

We see that under a high injection condition the carrier concentration at the front interface was just slightly modified by the applied gate voltage, but in this condition the influence of gate voltage becomes more efficient at two junctions, where the non-radiative Auger recombination dominates over the other mechanisms. Moreover, since electrons are more mobile compared to holes, the gate bias effect is stronger on the n^+/p junction than on the p^+/p junction, and this can be clearly seen in Figure 6.20a. When a negative voltage is applied to the gate, the decrease of the number of electrons at the n^+/p junction is larger than the increase of number of holes at the p^+/p junction, as a result the total Auger recombination in the whole device volume decreased. Whereas, at a positive gate voltage the growth of the number of electrons at the n^+/p junction is greater than the reduction of the number of holes at the other junction; therefore the total non-radiative Auger recombination enhanced. As soon as the non-radiative process is modified, the radiative process will react in an opposite trend. This can be observed from Figure 6.20b when the diode works at 4 mA and 5 mA of forward current.

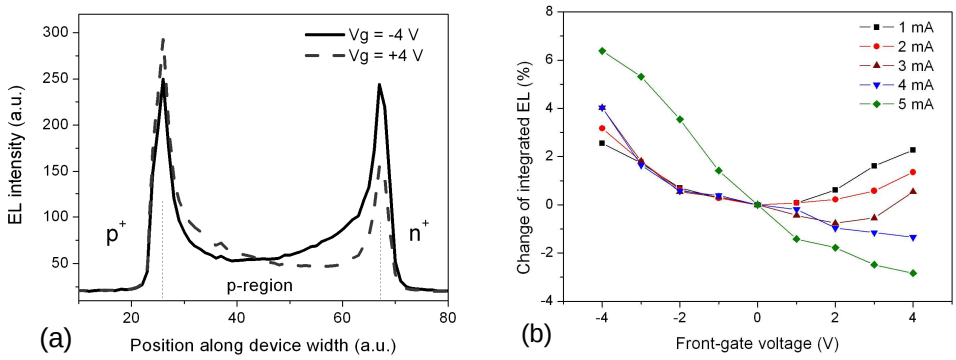


Figure 6.20: Field effects of front-gate voltage on EL profile of $p^+/p/n^+$ diode: (a) at 5 mA forward current, larger change of light intensity at the n^+/p junction; (b) change of integrated EL intensity at different current levels.

Moreover, we can also see that the relative relation of the non-radiative recombination process occurring at the interfaces and at the junctions depends on the injection level. This is shown in Figure 6.20b, the change of the integrated EL intensity depends on the injection. At a constant negative gate voltage, the integrated EL intensity increases with the injection level while an opposite trend was seen at a positive gate bias. It indicates that in this device the non-radiative recombination process at the interfaces keeps a stronger effect on device emission

than the contact recombination. Thus an opposite trend would be observed from the device where non-radiative recombination is more important at the contacts than that at the interfaces.

6.5 Two barrier structures

The LED structure with two thinned access silicon layers (Figure 6.2c, d) was proposed to yield a large improvement of the electroluminescence efficiency since there are three effects contributing to the carrier confinement in the emitting volume, which are:

- *Electrical field effects:* by administering the appropriate gate potential, minority carriers experience a potential barrier in this thin film;
- *Geometrical effects:* the injected carriers have difficulties in finding the exit through diffusion, as it is geometrically small;
- *Band-gap widening effects:* the minority carriers encounter an energy wall of the larger band-gap energy at the thinned silicon layer (as thickness below ca. 10 nm).

In the following paragraphs, these effects are identified experimentally and by simulations. All the experimental parameters of the optical and electrical characterization presented in the following were obtained from devices with the width of 60 μm. The simulation current was calculated (from the simulation current-density) for the structure with a 60 μm width.

6.5.1 Electrical characterization

Current-voltage (*I-V*) characteristics of devices are measured between the n^+ and p^+ region showing diode operation with a slope of 72 mV/decade. Holes and electrons are injected into the central area through the thinned regions. The access resistance of such diodes is high, and increases with a decrease of the thinned silicon region. The diode current strongly depends on the series resistance of the thinned layers. This series resistance can be reduced sufficiently by applying a bias-voltage to poly-gates on top of the thinned regions. By application of a negative voltage (V_{b1}) to the poly-gate next to the p^+ region and a positive voltage (V_{b2}) to the poly-gate next to the n^+ region, the carrier density in the thinned silicon layer is enhanced. From the structure in Figure 6.2c we observed that when V_{b1} = -1 V and V_{b2} = 1 V, the series-resistance was reduced by $\sim$4 times.

This leads to good forward conduction: at V_{b1} = -1 V and V_{b2} = 1 V, 1 mA flows at $\sim$2 V forward bias (V_F). Meaning that at enhanced condition, a V_F = 2 V can lead to a mean current density of 3.3 $\times$ 10^5 A/cm^2 through a silicon layer thinned down to 5 nm and a current density of 1.14 $\times$ 10^4 A/cm^2 through the central region. Figure 6.21 shows *I-V* characteristics of five diodes with varying thinned-region thickness.

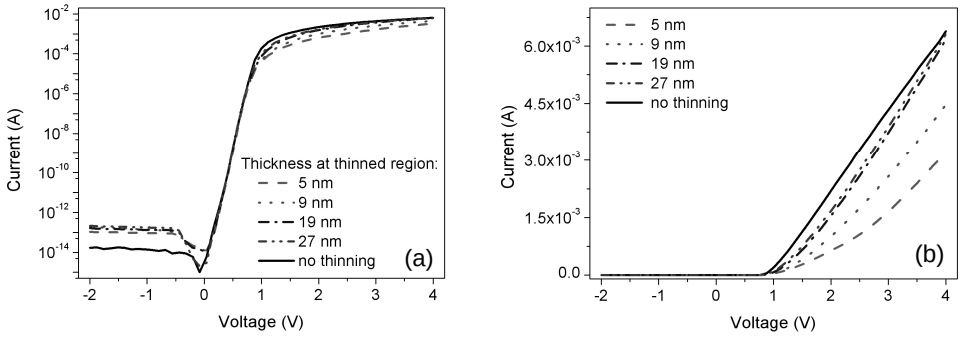


Figure 6.21: *I-V* characteristics of 5 diodes with the same structure except the thickness of the thinned region, measured at room temperature for V_{b1} = -1 V and V_{b2} = 1 V: (a) current in semi-log scale; and (b) current in linear scale. The 5 diodes in this measurement with the distance between the two thinned regions of 5 μm.

Since a larger band-gap certainly exists in a thinner entrance layer, it is not easy to separate the geometrical effects from the band-gap widening effects. Simulations enable us to decrease the thickness of the access layers while keeping the band-gap energy constant. It also opens the possibility to change the band-gap while keeping the access layer thickness at the same level. In order to study these two consequences separately we used simulation tools and it is presented in the luminescence property section.

6.5.2 Luminescence characterization

We compared the electroluminescence at room temperature of five diodes, which only differ in thickness of the thinned access silicon film. Their EL spectra with the same intensity-peak at $\sim$1130 nm wavelength are recorded in Figure 6.22a. The EL increases by as much as a factor 24 when access regions are thinned from 146 to 5 nm, as quantified by the integrated EL intensity in Figure 6.22b. This enhancement of electroluminescence in identical silicon volumes (on the same wafer), but with different access regions, is explained by confinement of the injected carriers in this volume. Three confinement effects to that enhancement will be identified as following.

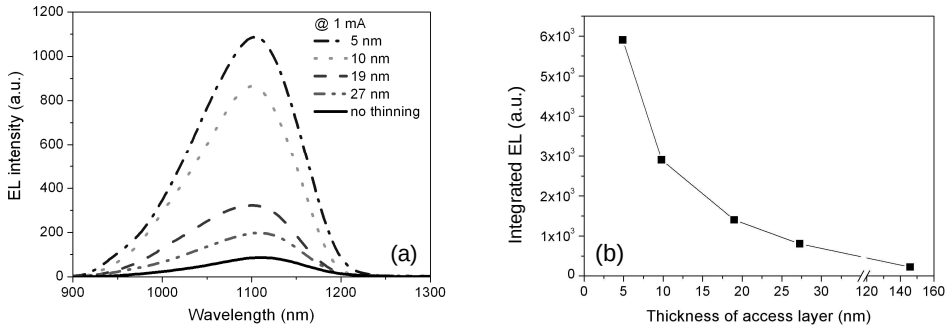


Figure 6.22: (a) EL spectra of five diodes with the same emission region volume (5 μm $\times$ 60 μm $\times$ 146 nm) but different access layer thickness measured at room temperature and under 1 mA forward current; (b) the integrated EL intensity of these diodes as a function of thinned SOI thickness.

The effect of gate voltages was studied on these fabricated diodes at the same forward-current of 500 μA, under two biasing conditions: first, with both poly-gates grounded and second, with gate biases of V_{b1} = -1 V and V_{b2} = +1 V. The latter condition creates a high electron density in the thin silicon region connected to the n^+ contact, and a high hole density in the thin film adjacent to the p^+ contact. Not only does this reduce the diode's external resistance; holes, injected into the p-type silicon now encounter a potential barrier on their way to the n^+ region, and similar for electrons, vice versa. The integrated EL intensity ratio between these two conditions increases from 1.5 to 2.5 when decreasing the thickness of the thinned regions from 27 to 5 nm respectively, as shown in Figure 6.23.

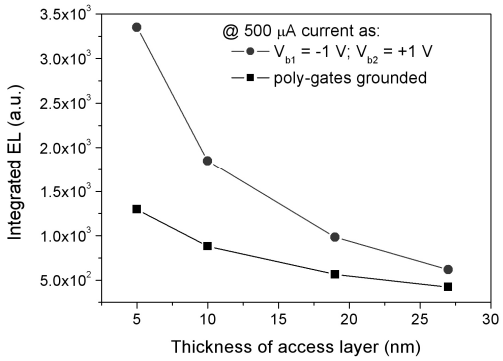


Figure 6.23: Comparison of the integrated EL intensity for diodes working under two bias conditions: two poly-gates grounded and biased at V_{b1} = -1 V and V_{b2} = +1 V.

The influence of gate-voltage at each poly-gate on the emission property was investigated further by a change in observation of integrated EL under a constant current when keeping one gate at constant bias while varying the applied voltage

at the other one, and vice versa. Figure 6.24 shows that the relative importance of both gates is almost equal. As soon as the access channels are driven to accumulated condition, the EL intensity is going to be at saturation. And it can also be observed that the introduced electrical-field starts to do its function at an earlier state: the integrated EL intensity starts to saturate when $V_{b1} \cong$ -0.5 V and $V_{b2} \cong 0.7$ V.

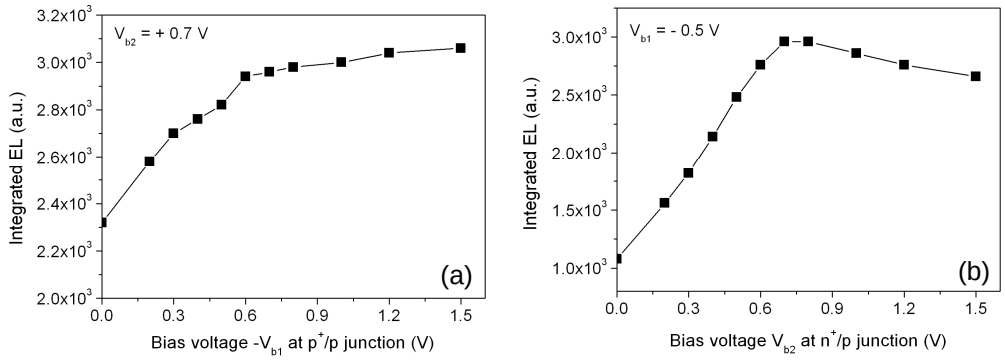


Figure 6.24: Change of integrated EL intensity with gate-voltage applied to: (a) V_{b1} while keeping V_{b2} at 0.7 V (at this bias level of V_{b2} the integrated EL starts to saturate); (b) V_{b2} while V_{b1} = -0.5 V (at this voltage of V_{b1} the integrated EL starts to saturate). The device has a 5 nm thick access layer and the forward current was 0.5 mA.

The EL improvement caused by electrical field effects was evaluated also by means of simulation of minority carrier current density within the thinned access layer at different applied gate-voltages under the same current level flowing through the diode. More minority carriers appearing in the thinned region indicate that they contribute less to the radiative recombination in the central active region, and more loss of them to non-radiative recombination at the contacts. Simulation data supported the experimental observation as we see less minority carriers for a higher bias-voltage at the poly-gate (see in Figure 6.25). From cross-section of the simulation structure if now we draw a cut-line across the 5 nm thick access layer we can see the minority current density belonging to that cut-line. Electron current density at the access layer close to p^+/p junction and hole current density close to n^+/p junction can be seen respectively in Figure 6.25a and 6.25b at different bias levels of the poly-gates. In this simulation the field effect gives 2.3 time-increase of the mean radiative recombination rate occurring in the central p-region.

Thinning down the access regions has a stronger effect (see Figure 6.22b and 6.23). In Figure 6.23, in the case of no field effect an EL increase of a factor 3 is observed when the access layer thickness decreases from 27 nm to 5 nm. While the quantum-size effect is known to be significant only when the silicon

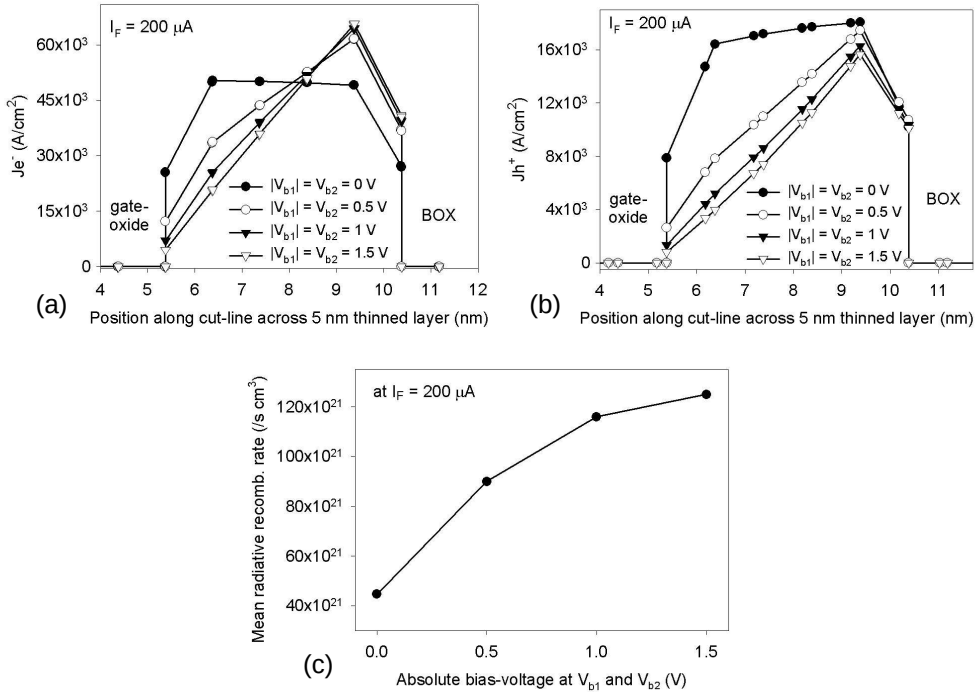


Figure 6.25: Simulation of the change of the minority current density within the 5 nm thick access Si layer versus the bias voltage at poly-gates while 200 μA current flowed through the device. At a higher gate-voltage of poly-gates: (a) less electrons can reach the p^+/p junction; (b) holes were rejected of reaching the n^+/p junction; (c) higher radiative recombination rate occurring within the central p-region.

layer thickness is below 10 nm [13] [14], we realize that the EL intensity starts to increase as the thinned silicon layer is still quite thick (27 nm and 19 nm). This is evidence of the geometrical effect.

The geometrical effect on EL can be analyzed separately by device simulation. In the input data of the simulation model, the silicon band-gap at the access region is kept at the same energy of 1.12 eV for all five thickness levels of 5, 9, 15, 30, and 150 nm. At the same forward current of 200 μA, thinning down of access layers helps to the confinement of electrons and holes in the central p-region and therefore increases radiative recombination probability. The radiative recombination rate along a cut-line across the device length with different thicknesses of the access-layer can be seen in Figure 6.26. We see two sharp peaks respectively at the two junctions, which is the result of the band-gap narrowing effect in highly doped silicon. There are two important points to be aware of here: firstly, the light emitted from these two peaks will be mostly absorbed back by the n^+ and p^+ region; secondly, the recombination simulations show rates per cubic and since

the non-thinned p-region is much thicker than the access layer, the integration of this radiative recombination rate across the thickness of the corresponding region show that the most effective part contributing to the device emission is the central non-thinned region. Therefore, in the remaining simulation data we just take into consideration the radiative recombination from the central p-region. It is shown in Figure 6.27 that the mean radiative recombination rate increases with a factor of 4.5 when the access-layer thickness decreases from 150 nm to 5 nm. Fewer electrons (holes) diffused through a thinner access layer to reach p^+/p (n^+/p) junction, leading to a higher radiative recombination rate in the central p-region. This once more indicates the stronger effect of geometrical thinning.

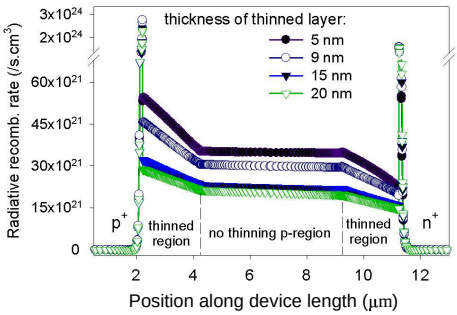


Figure 6.26: Simulation of contribution of radiative recombination rate along the device-length with different thickness of the thinned layer. Diode simulated at 200 μA with V_{b1} = V_{b2} = 0 V.

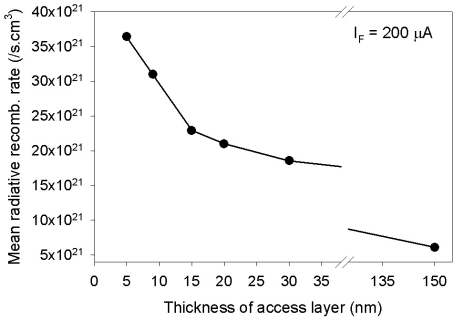


Figure 6.27: Mean radiative recombination rate within the central p-region as a function of the access-layer thickness. Diode simulated at 200 μA with V_{b1} = V_{b2} = 0 V.

The same simulation procedure was carried out to separately investigate the band-gap widening effect. In a structure with 9 nm thick access layer, we define the silicon band-gap of this access layer at different energies and compare the total recombination rate in the central emitting region. With the reported observation of the band-gap widening effect [13] [14], for a silicon layer of 5 ± 2 nm thick its band-gap can be widened up to 1.2 eV, so in our simulation the silicon band-gap of this thin layer was set at 1.12, 1.14, 1.17 and 1.2 eV. Because of the band-gap widening the carrier confinement process can be seen clearly in Figure 6.28. At the same simulated current of 200 μA, we see more carriers confined within the central region resulting into a higher band-to-band recombination rate when increasing the silicon band-gap of the access layer. The comparison of mean radiative recombination rate within the central p-region at different energy levels of silicon band-gap is performed in Figure 6.29. The band-to-band recombination rate is enhanced by 2.2 times with a 80 meV increase of the band-gap energy in the access region.

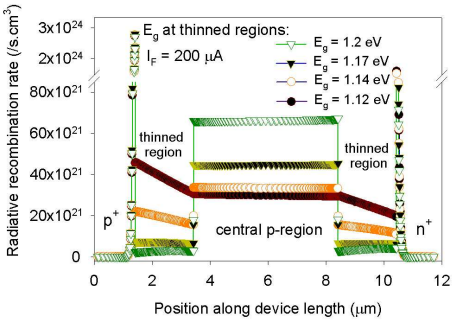


Figure 6.28: Simulation of contribution of radiative recombination rate along the device-length with different setting of silicon band-gap at the thinned layer. Diode simulated at 200 μA with $V_{b1} = V_{b2} = 0$ V.

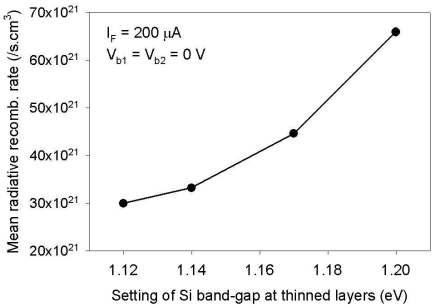


Figure 6.29: Mean radiative recombination rate within the central p-region increases with band-gap of the thinned access-layer. Diode simulated at 200 μA with $V_{b1} = V_{b2} = 0$ V.

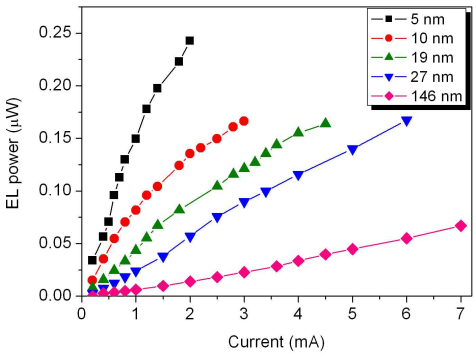


Figure 6.30: *L-I* characteristics of diodes measured at room temperature.

The simulation data presented above clearly distinguish three confinement effects implemented in our devices. And it indicates that the 24-time improvement of the external quantum efficiency, which was experimentally observed in our fabricated devices, is a reasonable result.

The *L-I* characteristics of those diodes at room-temperature are shown in Figure 6.30. Note that the surface of this device did not receive any special treatment to maximize the outcoupling of light [1]. The external quantum efficiency of the device at room temperature under 1 mA forward current reaches 1.4×10^{-4} for the device with the thinnest SOI layers (5 nm). According to our calculations of internal efficiency (presented previously in chapter 2), the highest possible internal efficiency in this geometrical is close to 1 % with the assumption of a surface recombination velocity s = 10 cm/s. Moreover, if we realize these devices on a thicker SOI layer (>2 μm), together with further improvement of Si/SiO_2 inter-

face quality, it would be possible to reach an internal efficiency level of 5 %.

Distribution and spatial location of the emitted light can be seen for example in Figure 6.31. It is a top-view infrared photograph of a device (with the access layer of 5 nm thick; the p-region of 10 μm long and 60 μm wide) biased at 1 mA taken by the InGaAs camera. The contact-pads and device structure is visible in this picture because we additionally illuminated the device by a weak external lamp. The bright central area is the active region (p-type peninsula); two brighter ends of the central area are a result of the part of internally reflected light waveguided to the edge at the proper escape angle. The two poly-gates adjacent to the central region, which control the access of carriers, also waveguide part of the emitted light in the direction of the p^+ and n^+ regions. Part of this escaped at the edges of the poly-silicon. In the case of the structure on the right-side of Figure 6.31, there is also a gate on top of the central p region and we see two brighter lines at the short edge of the device. One is due to the waveguiding in the SOI layer and the other one due to the waveguiding in the poly-gate on top of it. The integrated intensity from the edges amounts to 15-20 % of the total light emission. Moreover, one can still recognize that the emission on the right-side of centre region (p^+/p junction) is higher than that on the left-side (n^+/p junction), which is the same emission profile from the normal $p^+/p/n^+$ diode presented earlier.

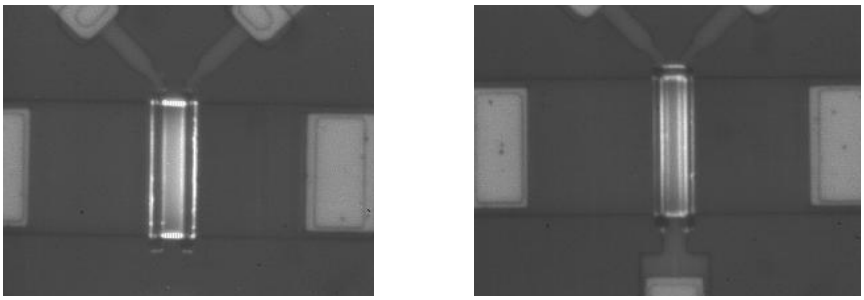


Figure 6.31: Top-view infrared photograph of the light emitting device biased at 1 mA, taken by InGaAs camera via a 50x-microscope: (left) no central gate; (right) with central poly-gate. The device has an access layer of 5 nm thick; the p-region is 10 μm long and 60 μm wide; at bias condition of V_{b1} = -1 V and V_{b2} = 1 V.

With the right-structure in Figure 6.31, it is possible to use the central poly-gate to further increase device-light-emission by limiting the non-radiative recombination occurring at the Si/SiO_2 interfaces. The external observation showed an EL increase of a few percentages as previously presented with the normal $p^+/p/n^+$ diodes. For our fabricated diodes the optimal voltage applied to the central gate is -4 V.

Temperature effects

The temperature dependence of the integrated EL intensity was investigated in the range of 253-473 K for all series of fabricated devices. An interesting temperature dependence of EL characteristics was observed, which indicated quantum confinement effects (see Figure 6.32). As far as the potential confinement is concerned (electrical field effect and/or band-gap widening effect) the EL intensity decreases with temperature. This was indicated by a decrease in the inte-

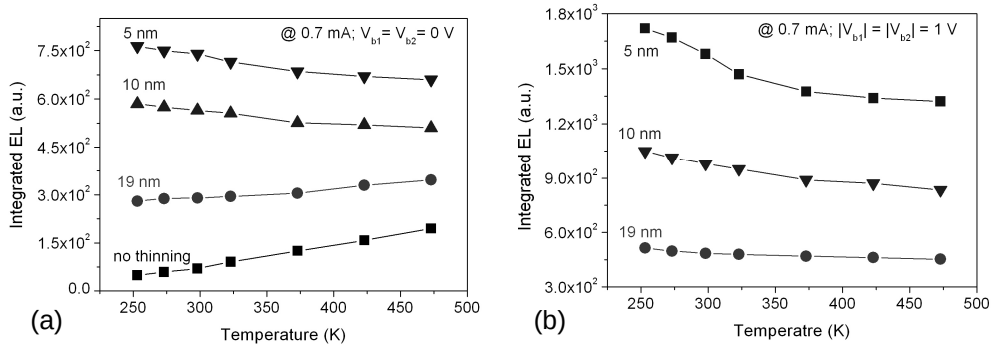


Figure 6.32: Temperature dependence of integrated EL intensity of diodes with different access layer thickness under 0.7 mA forward current when: (a) poly-gates are grounded or (b) poly-gates are biased of V_{b1} = -1 V and V_{b2} = 1 V.

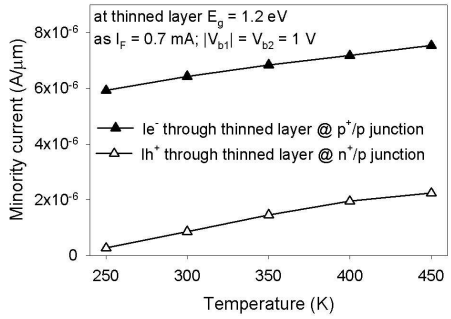


Figure 6.33: Under a constant current of 0.7 mA, with gate-bias of V_{b1} = -1 V and V_{b2} = 1 V; and silicon band-gap of the thinned layer of 1.2 eV, the integrated minority current density along the cut-line across the thinned layer increases when increasing temperature.

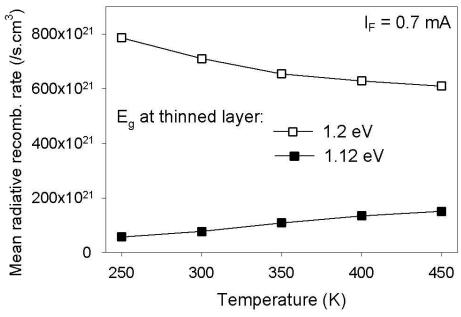


Figure 6.34: Temperature dependence of the integrated radiative recombination rate along device length for two different simulation conditions of band-gap energy at the thinned access regions: E_g = 1.12 eV (V_{b1} = V_{b2} = 0 V) and E_g = 1.2 eV (V_{b1} = -1 V and V_{b2} = 1 V).

grated EL intensity with temperature obtained from devices with the thinned region thickness smaller than 10 nm at both bias-conditions of poly-gates (grounded

or biased) and from devices with thicker access layers (>10 nm) when poly-gates were biased. The opposite trend, in line with bulk silicon LED behavior [23] [24], occurred for devices without thinning and with a thicker 10 nm thinned layer when two poly-gates grounded.

In confined-carrier systems, the confinement is normally reduced by increasing temperature [25] [26]. In our device, this happens through the increase of the minority carrier concentration in the thin regions at fixed gate potential. Thermal escape of carriers through quantum confinement barriers increased with temperature (Figure 6.33). Simulation data presented in Figure 6.34 clearly strengthens the observed experimental data. Under a constant current density of 7.8 $\times$ 10^4 A/cm^2 (0.7 mA), with the silicon band-gap energy at the thinned region was set to 1.2 eV, at the gate-bias of V_{b1} = -1 V and V_{b2} = 1 V, when increasing temperature from 250 K to 450 K we see the integrated EL intensity decreasing as a result of the increase of escaped carriers. Whereas, an opposite trend was observed when the band-gap was set to 1.12 eV and the gate-bias of V_{b1} = V_{b2} = 0 V.

The found temperature dependence behavior indicates that our devices work efficiently at around room temperature and above, allowing the utilization of this emission process in integrated microsystems.

Conclusion

A compact efficient light source on SOI material with many geometrical variations was presented. The devices emit infrared light based on phonon-assisted band-to-band recombination in high-quality silicon. Carrier confinement effects were successfully implemented. Using thinned down, gated silicon access regions, the quantum efficiency was shown to improve with almost two orders of magnitude.

The experimental results were compared with simulations and three carrier confinement effects were identified, i.e., electrical field, geometrical and quantum size effects. The combination of these effects resulted in a device which exhibited a record electroluminescence efficiency for SOI-LEDs.

Compared to bulk-silicon LEDs it has the advantage of a laterally and vertically well-defined light emitting area, and probably higher switching speed. The quantum efficiency can be enhanced further by improvement of the Si/SiO_2 interface quality and increase the relative recombination fraction between volume and interface components. The quantum effects can be more efficient with a thinner access layer (<5 nm).

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Chapter 7

Conclusions

Abstract

To finalize the thesis and the four-year project named HELIOS, the main goals are included in this chapter and the conclusions belonging to each chapter are summarized. From there some general conclusions are drawn. And finally, some future research is proposed.

7.1 Conclusions through the thesis

Chapter 2:

Based on the main possible recombination processes occurring in a silicon LED, the internal quantum efficiency of the luminescence processes (EL and PL) was calculated for a range of excess carrier concentrations from 10^{15} to 10^{19} /cm^3. The calculated data show that at low injection condition, when the SRH recombination is the dominant process, the impurity level (deep level impurities) is the most important parameter in both cases of bulk silicon LEDs or SOI-LEDs, which controls the fraction of the competing radiative band-to-band recombination rate to the total rate of all other non-radiative recombination processes. At a higher injection level the device efficiency is mainly limited by Auger recombination.

For the light emitting devices realized on SOI material, the non-radiative recombination at the interface and junctions is a key issue related to the device efficiency. To improve the light emitting efficiency, the non-radiative processes must be suppressed sufficiently. This can be done by limiting the contamination level during device fabrication processes, by improving the Si/SiO_2 interface quality, and by introducing a potential barrier to block electrons and holes from reaching the junctions.

Using the theory of optics and reported experimental data, a model was introduced to describe quantitatively the relation between external and internal efficiency of a light source. The relationship between internal and external efficiency of our realized light emitting devices was given by extraction from the built models. The influence of the backside reflection on the transmittance and the emission spectrum of the light sources realized on bulk silicon wafers is stronger compared to that of the light sources realized on SOI material.

Chapter 4 + 5:

The impact of dislocation loops on the infrared light emission from bulk silicon LEDs was studied. The p^+/n junction in the LEDs was fabricated using boron diffusion or boron implantation. The dislocation loops were created close to the p^+/n junction with different sizes, densities and at different positions by varying the implantation energy or post-implantation annealing temperature. The density and physical location of implantation-originating dislocation loops was confirmed by TEM and HRXRD measurements. Strong light emission is observed around the band-to-band recombination wavelength of 1150 nm, identified as phonon-assisted radiative recombination.

The BB radiation becomes progressively weaker at lower temperature, and with increasing dislocation loop density. This new finding contributes to a revision of the current understanding of light emission from defect-engineered silicon LEDs. In these experiments the presence of local carrier confinement close to dislocation loop regions due to the created strain field was NOT observed. From the found dependencies, it is concluded that with the applied manufacturing techniques (B diffusion, and B and Si implantation) the most efficient room-temperature silicon LED emitting at the band-to-band edge (1150 nm), is formed by causing minimum lattice damage.

D-band luminescence shows the opposite trend, both in temperature and the dislocation loop density. Ion-implanted silicon LEDs may present interest for light emission at 1.5 μm, however, to that purpose the dislocation loop density must be strongly increased compared to the devices presented here, while non-radiative recombination processes must remain suppressed.

Chapter 6:

A compact efficient light source on SOI material with many geometrical variations was presented. The devices emit infrared light based on phonon-assisted band-to-band recombination in high-quality silicon. Carrier confinement effects were successfully implemented. Using thinned down, gated silicon access regions, the quantum efficiency was shown to improve with almost two orders of magnitude.

The experimental results were compared with simulations and three carrier confinement effects were identified, i.e., electrical field, geometrical and quantum size effects. The combination of these effects resulted into a device which

exhibited a record electroluminescence efficiency for SOI-LEDs.

Compared to bulk-silicon LEDs, SOI-LEDs have the advantage of a laterally and vertically well-defined light emitting area, and probably higher switching speed. The quantum efficiency can be enhanced further by improvement of the Si/SiO_2 interface quality and increase the relative recombination fraction between volume and interface components. The quantum effects can be more efficient with a thinner access layer ($<$5 nm).

General conclusions:

The obtained results suggest the success of the HELIOS project.

In order to produce a high efficient Si LED, high quality silicon material and a low contamination level due to the fabrication process are two key issues. A $\sim$1 % internal quantum efficiency can be achieved with our SOI-LEDs. This closed the efficiency gap between bulk-Si LEDs and SOI LEDs. Moreover, this achievement opens a potential application for high speed photonic integrated circuits.

7.2 Future work

1. Performance of lateral SOI-LEDs with embedding few essential modifications in order to improve light emitting efficiency: use thicker SOI layer; create thinner access layers; control the contamination better during fabrication process. These possible variations are based on the theoretical predictions presented in chapter 2.

2. Investigate a complete optical integrated circuit including light-emitters, waveguide structures, and photodetectors. The light emitters are based on our high efficiency fabricated SOI LEDs. LPCVD Si_3N_4 with the band-gap energy of 4.6 eV and the refractive index of 2.05 is a suitable material for waveguiding signal through silicon integrated circuits. Furthermore, the LPCVD Si_3N_4 layer can be patterned by a CMOS compatible process.

3. Study the potential high switching speed of the SOI-LEDs using electrical and optical methods. External electrical field (by poly-gates) can be used to further increase the on/off switching frequency of the LEDs.

Summary

Since 1965 the number of transistors on a single integrated circuit (IC) for minimum component costs has been almost doubling each 18 months, a phenomenon which is known as Moore's law. The most advanced ICs contain more than a billion transistors and the line-width used in the next generation CMOS-processes is 32 nm. It is expected that in the coming decade the exponential increase in complexity will start saturating because we are approaching fundamental limits, and new approaches are being explored to push the development further after the saturation of conventional microelectronic technology. Instead of electrical interconnects, optical integration is suggested to be used in microelectronics. Furthermore, silicon nowadays remains the first material for IC technology. Meanwhile, a compact high-speed efficient silicon light source being suitable for on-chip integration process is still missing. The aim of this research is to investigate this missing component.

This dissertation presents an exploration on infrared-light emitting probability in silicon light emitting devices (Si-LEDs) with new approaches to improve the routinely low emission efficiency of silicon. It starts with a theoretical calculation of the possible internal quantum efficiency in bulk-Si LEDs and SOI-LEDs, after that a model for calculating the relationship between internal and external efficiencies is introduced. Following that the experimentally achieved results from our realized LED structures implementing the theoretical predictions are exhibited subsequently.

The probability ratio of radiative and non-radiative recombination in silicon determines the light emission efficiency of a Si-LED. The light emission from silicon is inefficient because the unwanted non-radiative recombination processes are faster than the desired radiative transitions of electrons and holes. The highest possible internal quantum efficiency of photoluminescence and electroluminescence for a bulk Si-LED and an SOI-LED is theoretically calculated in a wide range of excess carrier concentration from 10^{15}-10^{20} cm^3. This calculation shows that a high purity level of silicon wafer is required for a high efficient light source. Furthermore, the non-radiative recombination processes, such as Auger and Shockley-Read-Hall, occur mainly at the junctions and at the Si/SiO_2 interfaces. Thus, if one can inhibit the carriers from reaching these areas the radiative recombination will be enhanced consequently, i.e., the light emission efficiency is improved. Those information can be found in chapter 2 of this dissertation.

In chapter 3, the optical analysis equipment used in this work is described. Calibration of the optical system is an important issue to confirm the reliability of the obtained results. All information about the equipment used and procedures carried out in the calibration process of the optical system can be found in this chapter.

The importance of the purity of the silicon material is examined in the experimental series presented in chapter 4. The lattice defects were introduced in silicon wafer at different levels by implantation of either boron or silicon ions. When all device variations are realized on the same wafer the undesired variation from fabrication processes are excluded, the efficiency comparison of the emitted light between devices is made to investigate how dislocation-loops affect the light emission probability. A conclusion drawn from these experiments is that the Si-LEDs with less defects (high purity) will emit more light at the band to band wavelength of 1.15 μm. The created defects in silicon crystalline however do act as emitting centers at communications wavelength of 1.3-1.5 μm. These luminescence peaks are known as D-line emission (chapter 5). A wide range analysis of the dislocation-loop related emission is carried out at liquid nitrogen temperature (77.4 K) up to room temperature. It is shown that the band-to-band recombination and the D-line are competing each other, i.e., the D-line emission is stronger in the LEDs with more dislocation loops. However, the D-line emission caused by dislocation loops is negligible at room temperature, whereas, at a higher temperature the band-to-band emission is stronger.

Chapter 6 presents a new approach in which the limitations of bulk-Si LEDs caused by the lack of a spatial confinement; such as: low switching speed, difficulty in formation of compact optical integrated structures, cross-talk problems; can be improved by using SOI technology. The key element for that improvement is that the emitting region in our SOI-LEDs is a well confined area on a high quality SOI layer. An efficiency improvement of almost two orders compared to the reported thus far on SOI is the result of the successful utilization of carrier confinement effects in the realized SOI-LED structures. The way of using the standard local oxidation (LOCOS) technique to create two ultrathin access layers close to the p^+/p and n^+/p junction, respectively, in a p^+/p/n^+ structure is given. By doing that, three confinement mechanisms implemented at the same time in that emitting device are electrical field effects, geometrical effects, and band-gap widening effects. Simulation data supporting for those experimental results are also demonstrated in this chapter.

In conclusion, the success of this research project gives a contribution to the recent understanding of light emission from silicon and opens a highly potential application for high-speed photonic integrated circuits.

Samenvatting

Sinds 1965 is het aantal transistoren op een geïntegreerde schakeling (In het Engels Integrated circuit, afgekort IC) ongeveer iedere $1\frac{1}{2}$ jaar verdubbeld, een fenomeen dat bekend is onder de naam "wet van Moore". De meest geavanceerde IC's bevatten meer dan een miljard transistoren en in de komende generatie CMOS processen zullen afmetingen van 32 nm voorkomen. In de komende tien jaar verwacht men dat de exponentiële groei van de complexiteit zal afvlakken omdat de fundamenteel fysische grenzen bereikt zullen worden. Er zal gezocht moeten worden naar nieuwe benaderingen om de grenzen in de ontwikkelingen van de conventionele IC technologie verder te verleggen. Eén van de zaken waar onderzoek aan wordt verricht is om i.p.v. elektrische verbindingen, gebruik te maken van optische integratie terwijl toch silicium het basis materiaal voor dat soort ICs blijft.

Wat voor dat doel nog ontbreekt is o.a. een compacte supersnelle en efficiënte op silicium gebaseerde lichtbron. Het doel van dit onderzoek is het speuren naar deze ontbrekende schakel.

In dit proefschrift wordt onderzoek gepresenteerd naar de emissie van infrarood licht in silicium LEDs die gemaakt zijn via een nieuwe benadering om de gebruikelijke lage emissie efficiëntie van silicium te verbeteren. We beginnen met een theoretische berekening van de potentiële interne kwantum efficiëntie in bulk-Si LEDs en SOI-LEDs; daarna wordt een berekeningswijze gepresenteerd die handelt over de verhouding tussen interne en externe efficiëntie. Vervolgens worden experimentele resultaten, gemeten aan door ons gerealiseerde LED, gepresenteerd.

De verhouding tussen stralende en niet-stralende recombinatie in silicium bepaalt de hoeveelheid lichtemissie van een Si-LED. De lichtopbrengst in silicium is laag omdat ongewenste niet-stralende recombinatie processen sneller zijn dan de gewenste stralende recombinatie van elektronen en gaten. De hoogst mogelijke interne kwantumefficiëntie voor fotoluminescentie en elektroluminescentie van een bulk Si-LED and een SOI-LED is theoretisch berekend over een groot gebied (10^{15}–10^{20} cm^{-3})van lading injectie. Deze berekening laat zien dat een hoog zuiverheidniveau in een silicium plak een vereiste is voor een lichtbron met hoge efficiëntie. De niet-stralende recombinatie processen, zoals Auger- and Shockley-Read Hall recombinatie, vinden voornamelijk plaats bij de p^+p en n^+p overgangen en aan de Si/SiO_2 grensvlakken. Als men dus kan voorkomen dat de ladingsdragers deze overgangen bereiken zal als consequentie daarvan de stralende recombinatie toenemen. Dit wordt beschreven in hoofdstuk 2 van dit proefschrift.

In hoofdstuk 3 wordt de optische analyse apparatuur die in dit werk gebruikt is beschreven. Calibratie van het optische systeem is een belangrijk onderdeel om de betrouwbaarheid van de verkregen resultaten te garanderen. Alle informatie over

apparatuur en calibratieprocedures van het optische systeem kunt in dit hoofdstuk terugvinden.

Het belang van de zuiverheid van het silicium materiaal is onderzocht in een serie experimenten die beschreven staan in hoofdstuk 4. De rooster defecten werden op verschillende diepte niveaus geïntroduceerd in de silicium plak door implantatie van zowel borium als silicium ionen. Wanneer alle device variaties op dezelfde plak gerealiseerd worden, worden variaties in het fabricage proces uitgesloten. Een vergelijking van lichtopbrengst is gemaakt tussen verschillende devices om te zien hoe dislocaties licht emissie beïnvloeden. Een conclusie die uit deze experimenten getrokken kan worden is dat de Si-LEDs met minder defecten meer licht emitteren op de golflengte van 1150 nm, wat overeenkomt met de energieafstand tussen de conductieband en de valentieband (Eng. “band-to-band”). De gemaakte defecten veroorzaken echter een toenemende emissie bij de welbekende communicatie golflengtes van 1.3–1.5 μm. Deze luminescentie pieken zijn bekend als D-lijn emissie (hoofdstuk 5). Een veelomvattende analyse van de emissiegerelateerde dislocaties is uitgevoerd vanaf de vloeibaar stikstof temperatuur (77,4 K) tot aan kamertemperatuur. Het is duidelijk te zien dat de “band-to-band” recombinatie en de D-lijn recombinatie elkaar beconcurreren wat erop neerkomt dat de D-lijn emissie sterker is in LEDs met meer dislocaties. Echter de dislocatie gerelateerde D-lijn emissie is verwaarloosbaar bij kamertemperatuur terwijl de “band-to-band” emissie sterker is.

In hoofdstuk 6 wordt een nieuwe benadering getoond waarin de beperkingen van bulk Si-LEDs, die veroorzaakt worden door het afwezig zijn van ruimtelijke opsluiting van de ladingsdragers zoals: lage schakelsnelheid, het probleem van moeilijk te realiseren compacte optische geïntegreerde structuren en overspraak problemen, kunnen worden verbeterd door het gebruik van SOI technologie. Het belangrijkste element voor deze verbetering is dat de plaats van de emissie in onze SOI-LEDs in een goed gedefinieerd en opgesloten gebied plaatsvindt. Een verbetering van bijna 2 ordes van grootte is bereikt vergeleken met de tot dusver gerapporteerde resultaten op SOI. De manier waarop gebruik wordt gemaakt van standaard LOCOS techniek om twee ultradunne toegangslagen dicht bij de p^+/p, de n^+/p overgangen alsook in een $p^+/p/n^+$ structuur met ultra dunne p laag te realiseren wordt gepresenteerd. Hierdoor worden in het device drie opsluitingmechanismen tegelijkertijd doorgevoerd. Dat zijn elektrisch- veld, geometrischeen “band-gap” verbreding- effecten. Simulatie resultaten die deze experimenten ondersteunen worden in dit hoofdstuk ook weergegeven.

Tenslotte, dit onderzoeksproject levert een bijdrage aan de kennis van lichtemissie in silicium en geeft mogelijk aanleiding tot een toenemende toepassing van optische IC’s die bij hoge snelheid kunnen werken.

List of Publications

1. **Tu Hoang**, Phuong LeMinh, Jisk Holleman, Jurriaan Schmitz, *The Effect of Dislocation Loops on the Light Emission of Silicon LEDs*, IEEE Electron Device Letters, vol. 27, no. 2, pp. 105-107, February 2006.

2. P. LeMinh, **T. Hoang**, J. Holleman, J. Schmitz, *Influence of Interface Recombination in Light Emission from Lateral Si-based Light Emitting Devices*, ECS Transactions, vol. 3, no. 11, pp. 9-16, 2006.

3. **Tu Hoang**, Phuong LeMinh, Jisk Holleman, Jurriaan Schmitz, *Strong Efficiency Improvement of SOI LEDs through Carrier Confinement*, IEEE Electron Device Letters, vol. 28, no. 5, pp. 383-385, May 2007.

4. **Tu Hoang**, Jisk Holleman, Phuong LeMinh, Jurriaan Schmitz, Teimuraz Mchedlidze, Tzanimir Arguirov, and Martin Kittler, *Influence of Dislocation Loops on the Near-Infrared Light Emission from Silicon Diodes*, IEEE Transactions on Electron Devices, vol. 54, no. 8, pp. 1860-1866, August, 2007.

5. J.-L.P.J. van der Steen, R.J.E. Hueting, G.D.J. Smit, **T. Hoang**, J. Holleman and J. Schmitz, *Valence band offset measurements on Thin Silicon Double-Gate MOSFETs*, IEEE Electron Device Letters, vol. 28, no. 9, pp. 821-824, September 2007.

6. **T. Hoang**, P. LeMinh, J. Holleman, J. Schmitz, H. Wallinga, *High External Quantum Efficiency of the Lateral P-I-N Diodes Realized on Silicon On Insulator (SOI) Material*, Proceedings of SAFE 2003, the 6th Workshop on Semiconductor Advances for Future Electronics and Sensors, Netherlands, 23-24 November, 2003.

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8. **T. Hoang**, P. LeMinh, J. Holleman, V. Zieren, M. J. Goossens, J. Schmitz, *A High Efficiency Lateral Light Emitting Device on SOI*, Proceedings of EDMO 2004, 12th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications, South Africa, 8-9 November, 2004.

9. **T. Hoang**, P. LeMinh, J. Holleman, J. Schmitz, *The Effect of Dislocation Loops on the Light Emission of Silicon LEDs*, Proceedings of ESSDERC

2005, 35th European Solid-State Device Research Conference, Grenoble, France, 12-16 September, 2005.

10. P. LeMinh, **T. Hoang**, J. Holleman, and J. Schmitz, *The Effect of an Electric Field on a Lateral Silicon Light-Emitting Diode*, Proceedings of SAFE 2005, the 8th Workshop on Semiconductor Advances for Future Electronics and Sensors, Netherlands, 23-24 November, 2005.

11. P. LeMinh, **T. Hoang**, J. Holleman, J. Schmitz, *Influence of Interface Recombination in Light Emission from Lateral Si-based Light Emitting Devices*, Proceedings of ECS Meeting 2006, the 210th Meetings of the ElectroChemical Society, Cancun, Mexico, 29 October - 3 November, 2006.

12. T. Mchedlidze, T. Arguirov, M. Kittler, **T. Hoang**, J. Holleman, P. LeMinh, and J. Schmitz, *Engineering of Dislocation-Loops for Light Emission from Silicon Diodes*, Proceeding of GADEST 2007, XII Gettering and Defect Engineering in Semiconductor Technology Conference, October 2007.

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Biography

Hoang Tu was born in Viet Tri, Phu Tho, Vietnam on December 25th, 1974. In 1995 he received his BCs. degree in Physics at Physics Department, Pedagogy University of Hanoi 2, Vinh Phuc. After graduation, he worked at Physics Department of the same university as a lecturer's assistant with the task of education methods and skills on the field of Classical Mechanics.

In 2000 he received his MSc. degree in Materials Science at International Training Institute for Materials Science (ITIMS), Hanoi, Vietnam. His final MSc. assignment dealt with studying influence of synthesis method and substitute elements on negative electrode-material property of rechargeable Ni-MH battery. He continued to work at ITIMS after graduation with a research fellow till March 2003. The research focused on fabrication and characterization of giant magnetostrictive materials (Terfenol-D composite materials), and its possible applications on transducers and actuators.

April 2003, he came to work at Semiconductor Components Group in MESA+ Institute for Nanotechnology, University of Twente, The Netherlands with a scholarship from Vietnamese government. In October 2003, he started his Ph.D project funded by STW (Dutch Technology Foundation) at the same group. He has successfully realized new light-emitting-device structures on SOI (Silicon-On-Insulator) wafers with a highly potential application for on-chip integrations because of its high efficiency and high switching speed. His education task is assisting students with Silvaco simulations on IC-Technology and Devices. He finished his dissertation titled "High Efficient Infrared-Light Emission from Silicon LEDs" in September 2007.

Appendix A: Optical constants of some materials

In the fundamental optical regime, there are several different formulations of optical constants [C2.20]*. Based on the quantum-mechanical theory of absorption, Forouhi and Bloomer in [C2.20] built a series of general equations to derive the optical constants. The optical constants extracted from these equations show a good fit to experimental data. The wavelength dependence of the optical constants of intrinsic Si and SiO_2 used in this thesis were extracted from them. Therefore, in this appendix we introduce those expressions instead of simply referring to them as a reference.

To deduce these expressions the distinguishable states were defined as either the bonding and anti-bonding states in the valence band and conduction band of amorphous materials as $|\sigma\rangle$ and $|\sigma^*\rangle$, respectively. And for crystalline semiconductors, dielectrics, and metals the distinguishable states were defined as critical-point states, $|\kappa_{\mathrm{crit}}\rangle$, in the valence and conduction bands. The electron wave vector is presented as symbol κ.

The inter-band transitions of bound electrons are responsible for optical properties of a material. The relationship of photon (with energy $E = \hbar\omega$) absorption and electron transitions were studied to derive the extinction coefficient. After that, from the obtained equation for the extinction coefficient, the Kramers-Kronig relation was used to derive the refractive coefficient.

A.1 Derivation of extinction coefficient

The extinction coefficient for each material (amorphous, crystalline semiconductors, or metals) can be written compactly in following formulas.

For amorphous:

$$k_\alpha(\omega) = \frac{A(E - E_g)^2}{E^2 - BE + C} \tag{A.1}$$

with A, B, and C are constants given by:

$$A = const\,|\langle\sigma^*\,|\times|\,\sigma\rangle|^2 \times \gamma, \tag{A.2}$$

$$B = 2\,(E_{\sigma^*} - E_\sigma)\,, \tag{A.3}$$

$$C = (E_{\sigma^*} - E_\sigma)^2 + \frac{\hbar^2\gamma^2}{4} \tag{A.4}$$

*ref. [20] of Chapter 2

with $\gamma = 1/\tau$ and τ is the life-time of electrons at the excited state. In the Eq. (A.2), the term $|\langle\sigma^*|\times|\sigma\rangle|^2$ represents the dipole matrix element squared between the states.

For crystalline semiconductors and dielectrics:

$$k_\chi(\omega) = \left[\sum_{i=1}^{q} \frac{A_i}{E^2 - B_i E + C_i}\right](E - E_g)^2 \tag{A.5}$$

where the subscript *i* denotes the i^{th} type of the critical-point state, and the integer *q* is equal to the number of observed peaks associated with the critical-point transitions.

For metals:

$$k_\mu(\omega) = \left[\sum_{i=1}^{q} \frac{A_i}{E^2 - B_i E + C_i}\right](E)^2 \tag{A.6}$$

with A_i, B_i, and C_i are constants given by

$$A_i = const\,|\langle\kappa^c_{\text{crit}}|\times|\kappa^v_{\text{crit}}\rangle|^2_i \times \gamma_i \tag{A.7}$$

$$B_i = 2\left[E_c(\kappa_{\text{crit}}) - E_v(\kappa_{\text{crit}})\right]_i \tag{A.8}$$

$$C_i = \left[E_c(\kappa_{\text{crit}}) - E_v(\kappa_{\text{crit}})\right]^2_i + \frac{\hbar^2\gamma_i^2}{4} \tag{A.9}$$

where the superscripts v and c denote valence and conduction band, respectively. In Eq. (A.7), the term $|\langle\kappa^c_{\text{crit}}|\times|\kappa^v_{\text{crit}}\rangle|^2_i$ represents the dipole matrix element squared between the i^{th} critical-point state of the valence band and that of the conduction band.

A.2 Derivation of refraction coefficient

The refraction coefficients of a medium are expressed as the formulas.

For amorphous:

$$n_\alpha(\omega) = n_\alpha(\infty) + \frac{B_\alpha E + C_\alpha}{E^2 - BE + C} \tag{A.10}$$

where B_α and C_α are

$$B_\alpha = \frac{A}{Q}\left(-B^2/2 + E_g B - E_g^2 + C\right) \tag{A.11}$$

$$C_\alpha = \frac{A}{Q}\left[\left(E_g^2 + C\right)B/2 - 2E_g C\right]. \tag{A.12}$$

For crystalline semiconductors and dielectrics:

$$n_\chi(\omega) = n_\chi(\infty) + \sum_{i=1}^{q} \frac{B_{\chi i}E + C_{\chi i}}{E^2 - B_i E + C_i} \tag{A.13}$$

where $B_{\chi i}$ and $C_{\chi i}$ are

$$B_{\chi i} = \frac{A_i}{Q_i}\left(-(B_i)^2/2 + E_g B_i - E_g^2 + C_i\right), \tag{A.14}$$

$$C_{\chi i} = \frac{A_i}{Q_i}\left[\left(E_g^2 + C_i\right) B_i/2 - 2E_g C_i\right]. \tag{A.15}$$

For metals:

$$n_\mu(\omega) = n_\mu(\infty) + \sum_{i=1}^{q} \frac{B_{\mu i}E + C_{\mu i}}{E^2 - B_i E + C_i} \tag{A.16}$$

where $B_{\mu i}$ and $C_{\mu i}$ are

$$B_{\mu i} = \frac{A_i}{Q_i}\left(-(B_i)^2/2 + C_i\right), \tag{A.17}$$

$$C_{\mu i} = \frac{A_i B_i C_i}{2Q_i} \tag{A.18}$$

with Q_i is the same for crystalline semiconductors and metals as

$$Q_i = \frac{1}{2}\left(4C_i - B_i^2\right)^{1/2}. \tag{A.19}$$

A.3 $k(\omega)$ and $n(\omega)$ of Si and SiO_2

All parameters of A_i, B_i and C_i are obtained by fitting from experimental data [C2.20] for Si and SiO_2 as presented in Table 1 and 2 respectively. Applying these parameters to Eq. A.5 and Eq. A.13 the extinction coefficient as well as the refractive index of Si and SiO_2 as a function of wavelength can be extracted.

For crystalline silicon:

A_i	B_i (eV)	C_i (eV^2)	$n(\infty)$	E_g (eV)
0.00405	6.885	11.864	1.950	1.06
0.01427	7.401	13.754		
0.06830	8.634	18.812		
0.17488	10.652	29.841		

Table 1: Value of the parameters A_i, B_i and C_i for crystalline Silicon were extracted by fitting of experimental data. These parameters were extracted from [C2.20].

For silicon dioxide:

A_i	B_i (eV)	C_i (eV^2)	$n(\infty)$	E_g (eV)
0.00867	20.729	107.499	1.226	7.00
0.02948	23.273	136.132		
0.01908	28.163	199.876		
0.01711	34.301	297.062		

Table 2: Value of A_i, B_i and C_i for SiO_2 were obtained by fitting of experimental data. These parameters were extracted from [C2.20].

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